Repair Manual

SAMSUNG FACSIMILE

SF-330/331P/335T

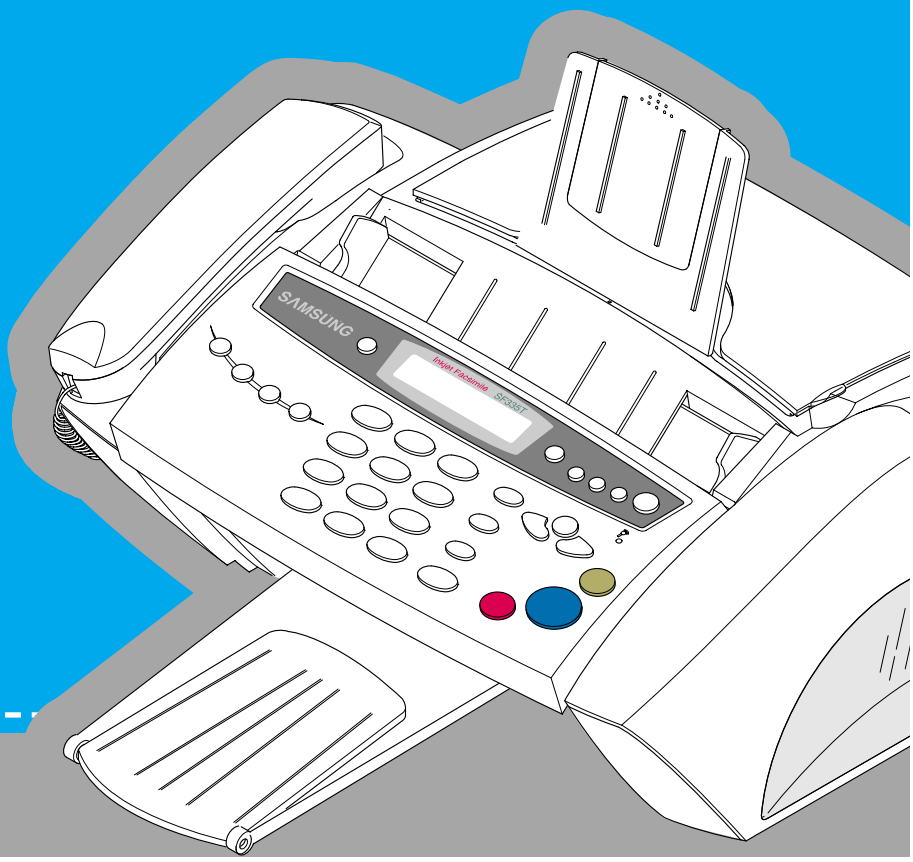
C•O•N•T•E•N•T•S

1. Block Diagram

2. Connection Diagram

3. Circuit Description

4. Schematic Diagrams



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SAMSUNG

This manual is made and described centering around circuit diagram and circuit description needed in the repair center in the form of appendix.

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CS Group

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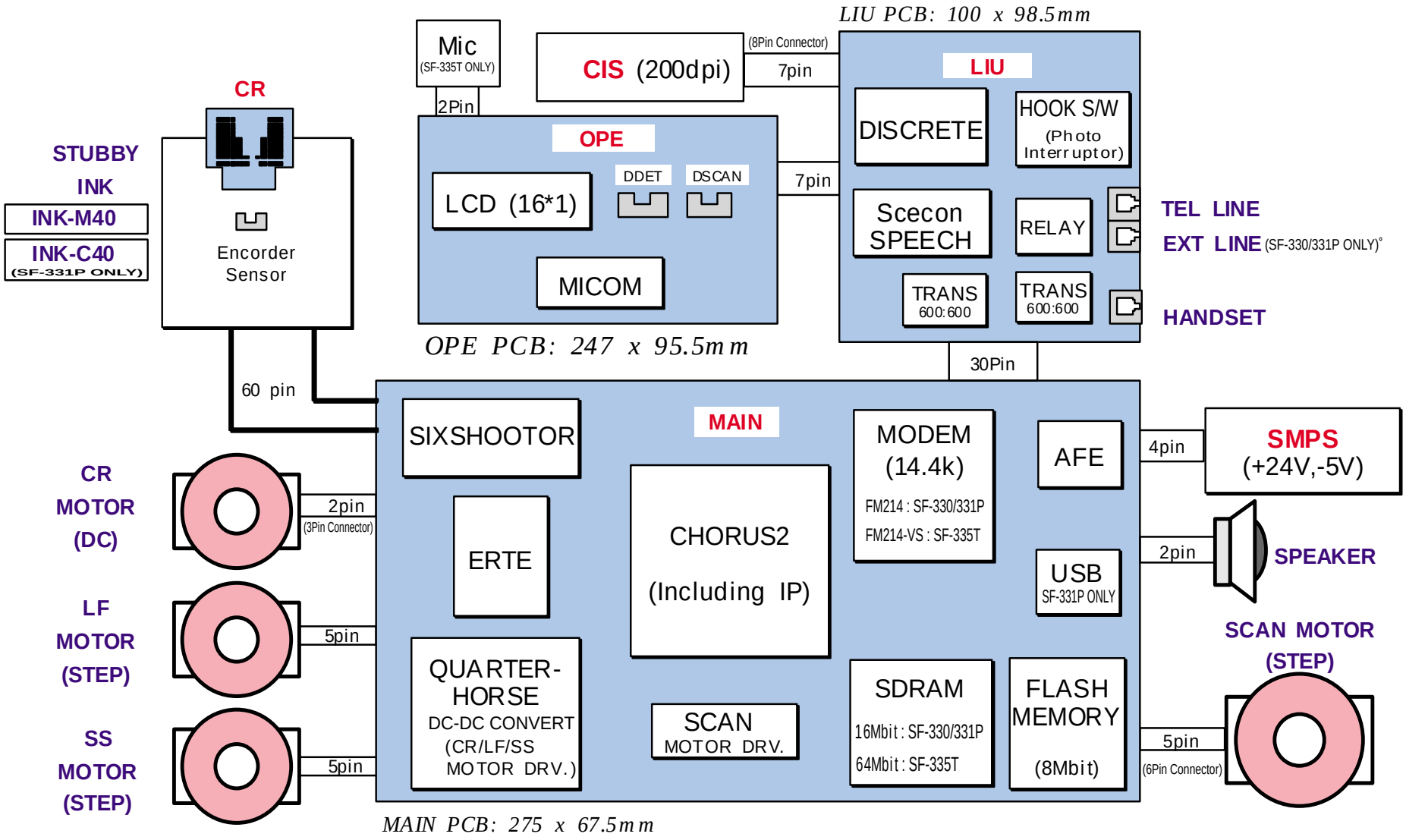
1. Block diagram



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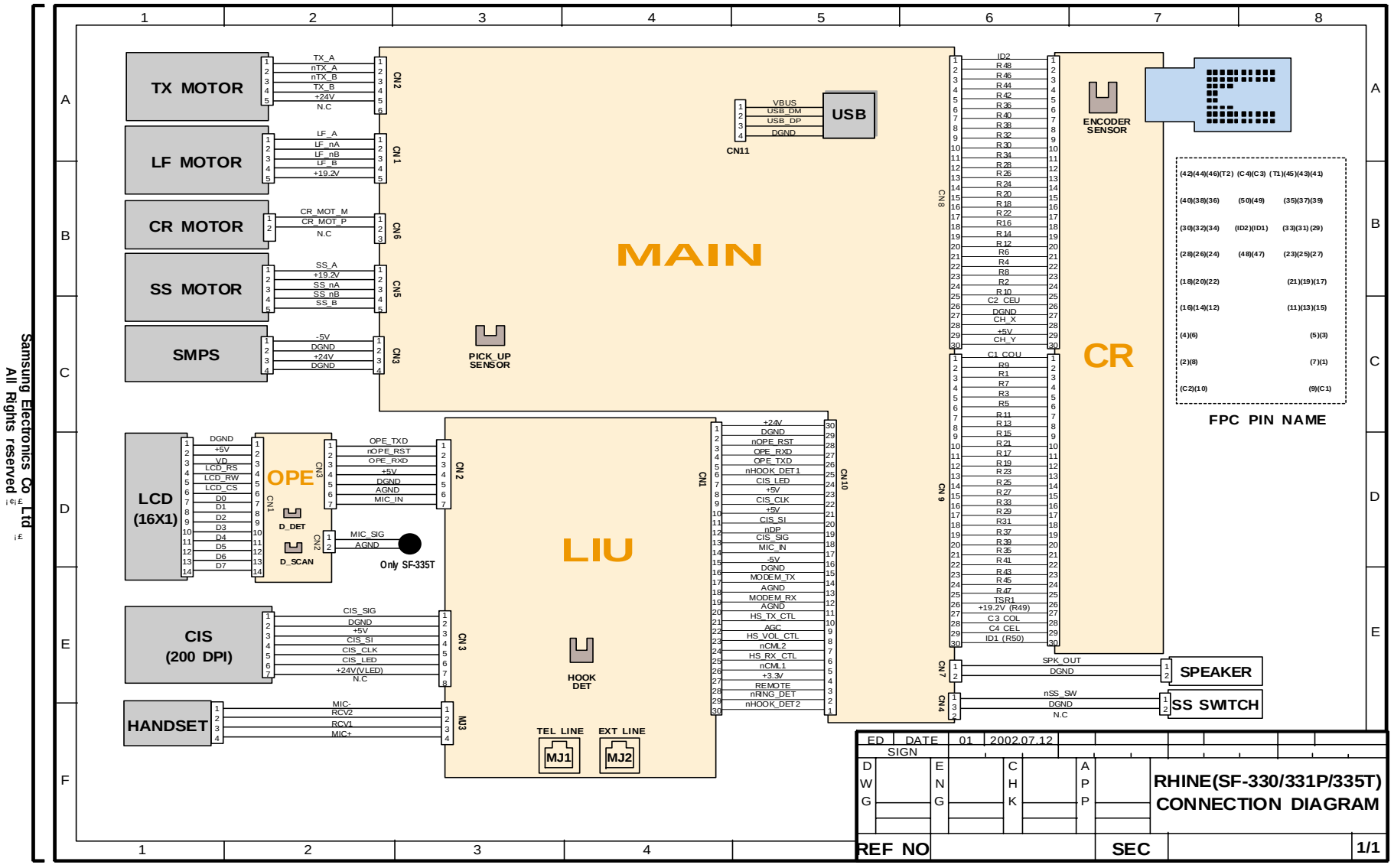
2. Connection Diagram



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3. Circuit Description

3.1 Main B'D

3.1.1 GENERAL DESCRIPTION

Main circuit consists of mainly consists of CPU and the controller part with various types of built-in I/O device driver(built-in RISC Processor Core : ARM7TDMI), system memory part, Image control part (CHORUS-2) controlling input of image received from media and conversion. The following nomenclatures by section is the same as those listed in the circuit diagram.

3.1.2 MEMORY MAP

The entire Addressing area provided by MAIN CONTROLLER(S3C46Q0X) is 256MBytes from 0x00000000 to 0x10000000, and the Max. Address Range for each External Chip Select is 32M Byte or Half word from 0x000000 to 0x01FFFFFF and embodied with Big-Endian Bus interface. MEMORY area is divided into EXTERNAL ROM and RAM areas(See (Figure 1)), and the areas actually used are 2M/8M BYTES SDRAM and 1M BYTES ROM(FLASH MEMORY). In case of SDRAM0, it uses 0x0000000h ~ 0x01BFFFFFh area.

0x0FFF_FFFF (32MB) 0x0E00_0000	Reserved Area 5
0x0DFF_FFFF (32MB) 0x0C00_0000	nSCS0 SDRAM(0) Area (2MB used - BASIC) (8MB used - TAD)
0x0BFF_FFFF (32MB) 0x0A00_0000	Reserved Area 4
0x09FF_FFFF (32MB) 0x0800_0000	Reserved Area 3
0x07FF_FFFF (32MB) 0x0600_0000	Reserved Area 2
0x05FF_FFFF (32MB) 0x0400_0000	Reserved Area 1
0x03FF_FFFF (32MB) 0x0200_0000	nGCS 1 MODEM Area
0x01FF_FFFF (4MB) 0x01C0_0000	Special Registers
0x01BF_FFFF (28MB) 0x0000_0000	nGCS 0 FLASH Area (1MB used)

<Figure 1. S3C46Q0X MEMORY MAP>

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3.1.3.1 BLOCK DIAGRAM and MAIN CONTROLLER description

<1> General description

MAIN CONTROLLER(S3C46Q0X,U12) consists of this system consists of CPU(ARM7TDMI RISC PROCESSOR), 8K BYTES CACHE, DATA and ADDRESS BUS, PLL deriding input frequency and CLOCK CONTROL part, SERIAL COMMUNICATION part supporting UART, PRINT HEAD control part, PARALLEL PORT INTERFACE part, USB INTERFACE part, Internal Image Processor Part, External DMA part MEMORY and EXTERNAL BANK control part, SYNCHRONOUS SERIAL INTERFACE control part for interfacing Quarter_Horse, and TX Motor drive control and general purpose I/O control parts.**(See Figure 2)**

3.1.3.2 S3C46Q0X FUNCTION DESCRIPTION

<1> SYSTEM CLOCK

There are two ways of Clock input method. One is the method to make Master Clock(MCLK) at the internal PLL by connecting X-tal and Capacitor to the outside, and another method is to use MCLK(When inputting 40MHz) directly, which supplies maximum 40MHz Clock to the EXTCLK terminal(PIN65). The range of frequency being input in case of using X-tal is limited to 4MHz~10MHz. For making the MCLK, the Clock is supplied to the EXTCLK Terminal of the ASIC by sending output power (32.256MHz) of the MODEM (FM214 or FM214-VS, U16) XCLK via the RC Filter. The inner side of the ASIC takes the Clock, and it goes to the MPLL circuit to create a basic operating frequency (66MHz MCLK signal). Also the Clock goes to the UPLL circuit to make the operating frequency of the USB Controller (48MHz).

<2> DATA and ADDRESS BUS CONTROL

1. _RD & _WR

_RD & _WR SIGNAL are synchronized with the inside MCLK(66MHZ) and becomes active to Low.

These signal are Strobe Signal used to Read or Write data when each Chip Select becomes active connected to SDRAM, ROM(Flash), _WR PIN, _RD of Modem.

2. CHIP SELECT
(_ROMCS, _IP_CS,_MED_CS,_SCS0,_SCS1)

- _ROMCS : FLASH MEMORY(U7) CHIP SELECT (LOW ACTIVE)
- _MODEM_CS : MODEM(U16) CHIP SELECT (LOW ACTIVE)
- _SCSO : SDRAM (BASIC 16MBIT(U9), TAD 64MBIT(U8), CHIP SELECT (LOW ACTIVE)

In case each Chip Select is low, it may Read or Write data.

3. D0 ~ D15

- 16BIT DATA BUS

4. A0 ~ A24

- ADDRESS BUS (A23 ~ A24 RESERVED)

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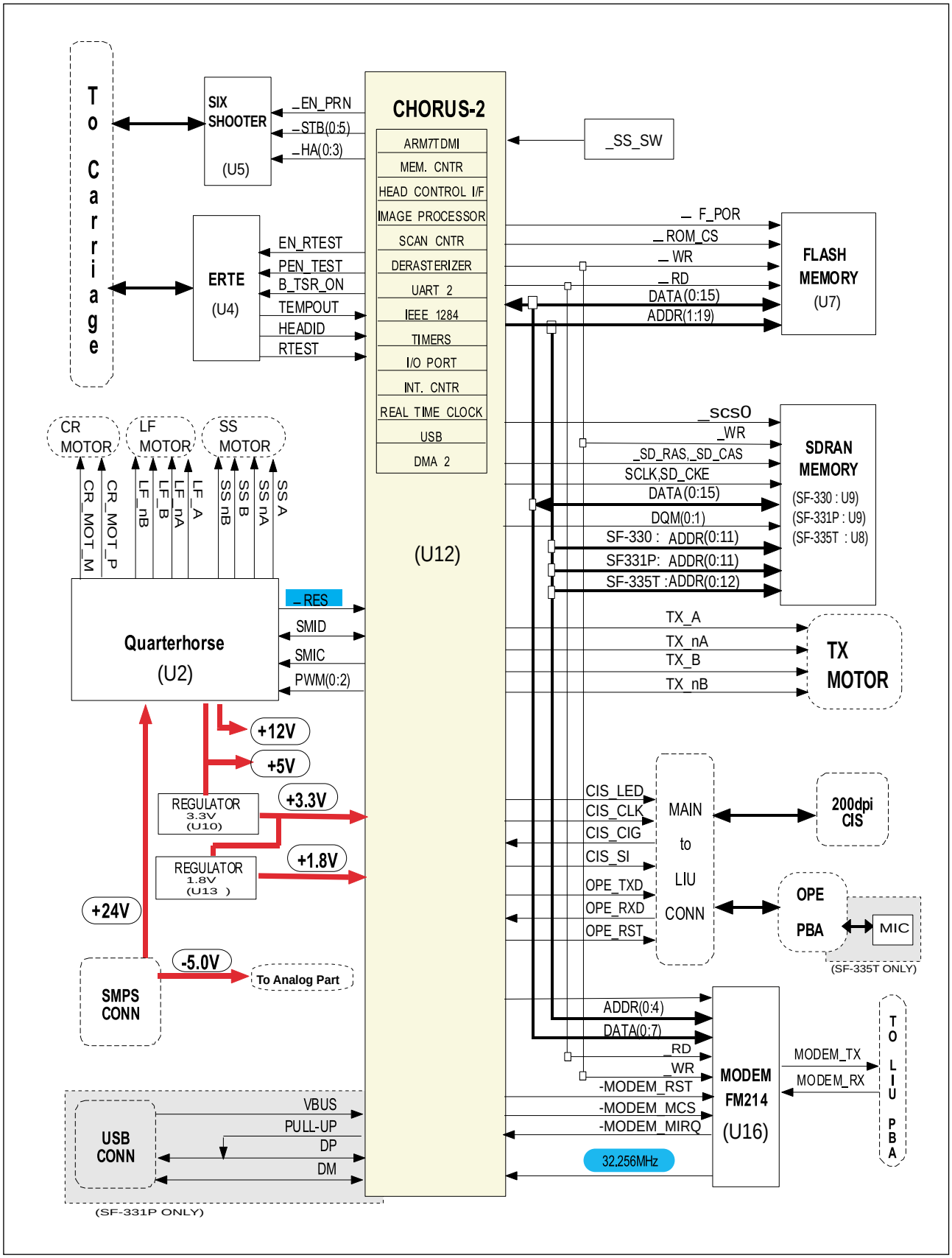

<Figure 2. Main Part Interface Signals>

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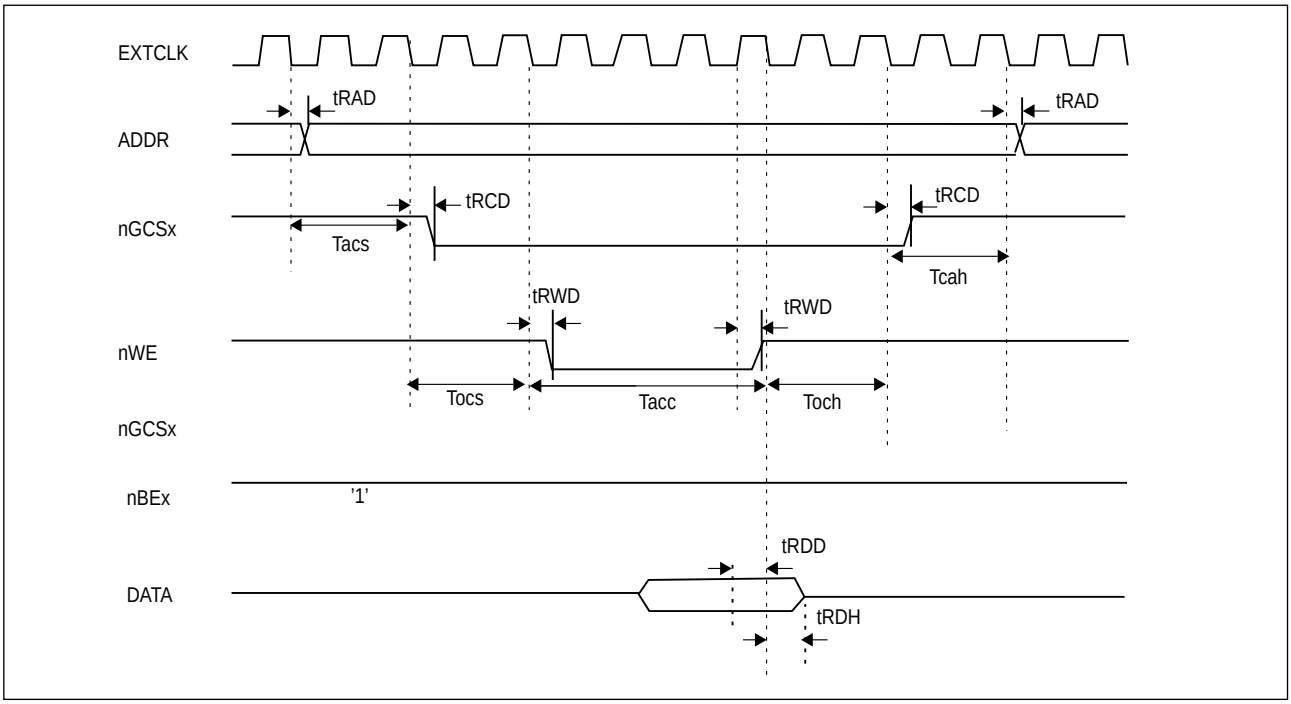
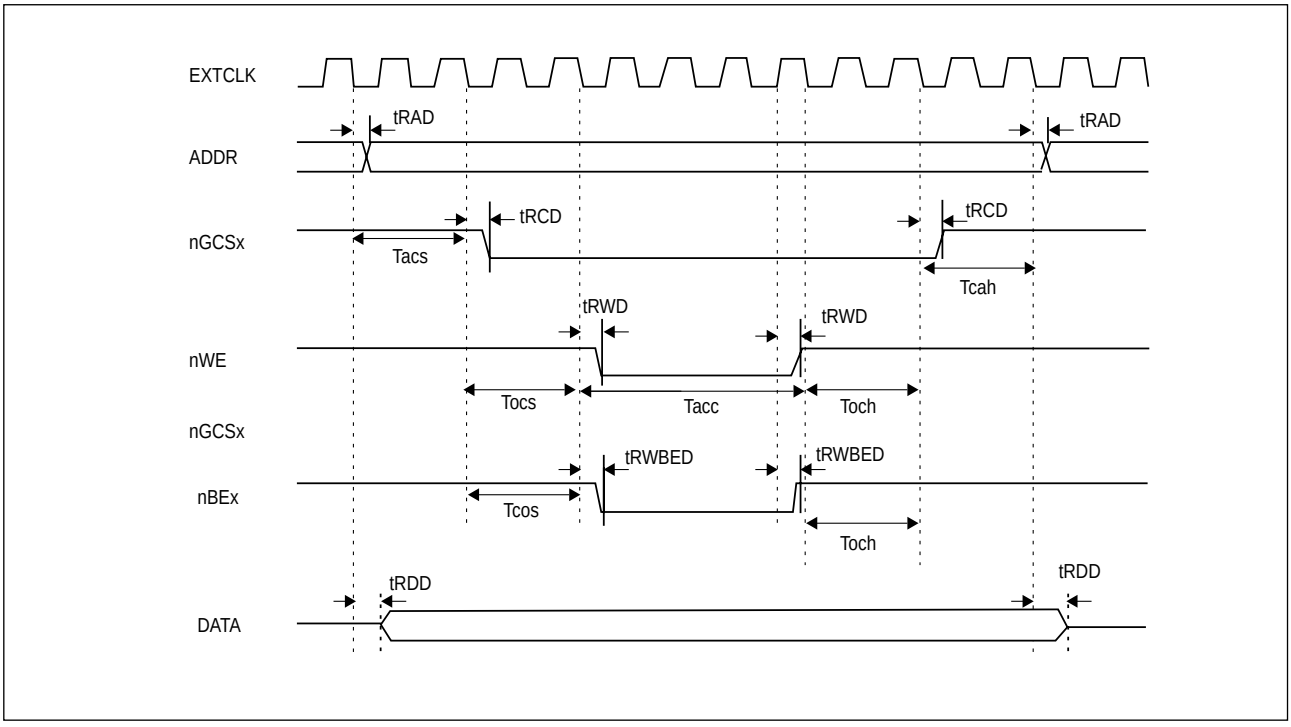


<Figure 3. Flash Memory Read Timing>



<Figure 4. Flash Memory Write Timing>

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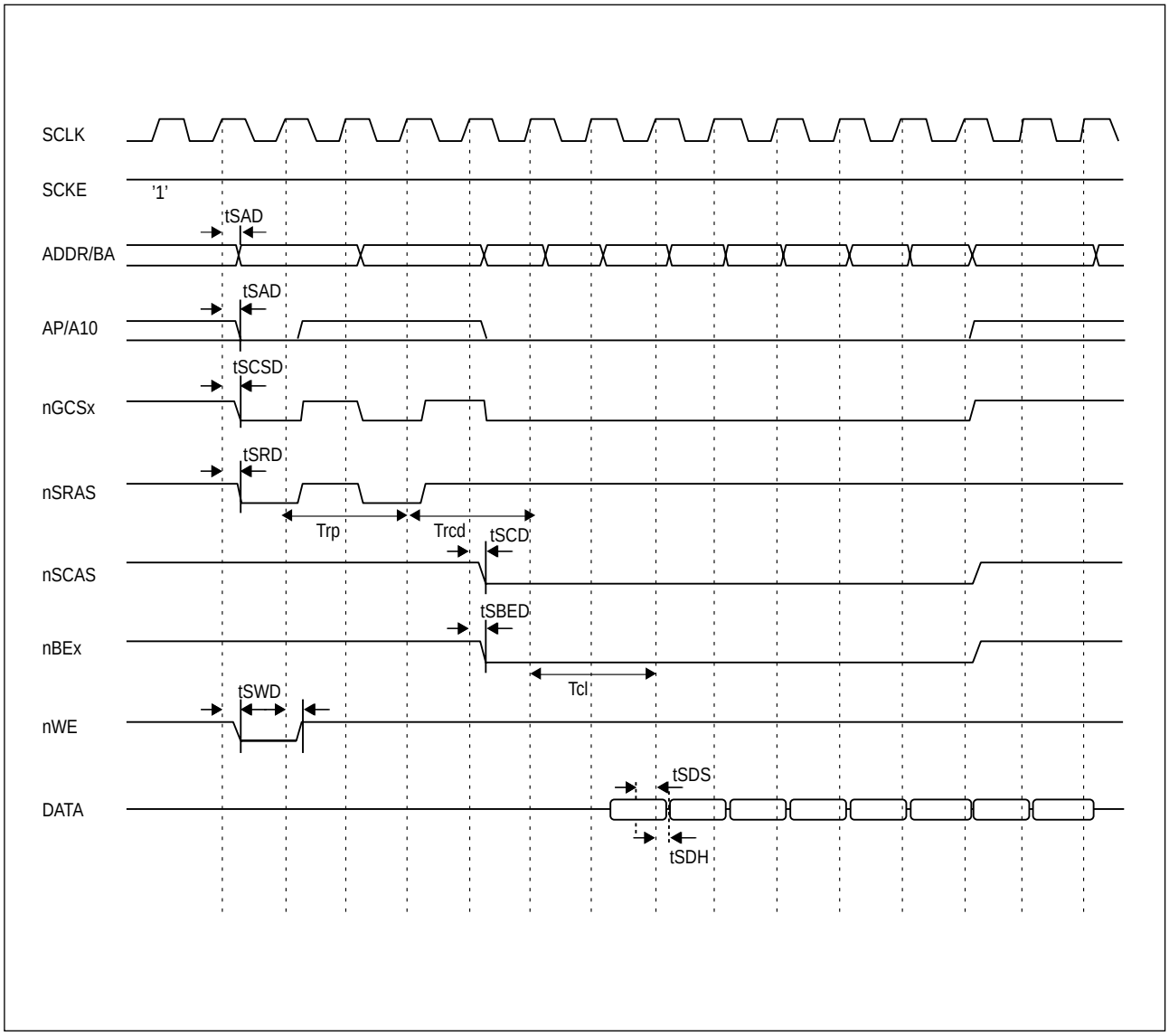

<Figure 5. SDRAM Read Timing>

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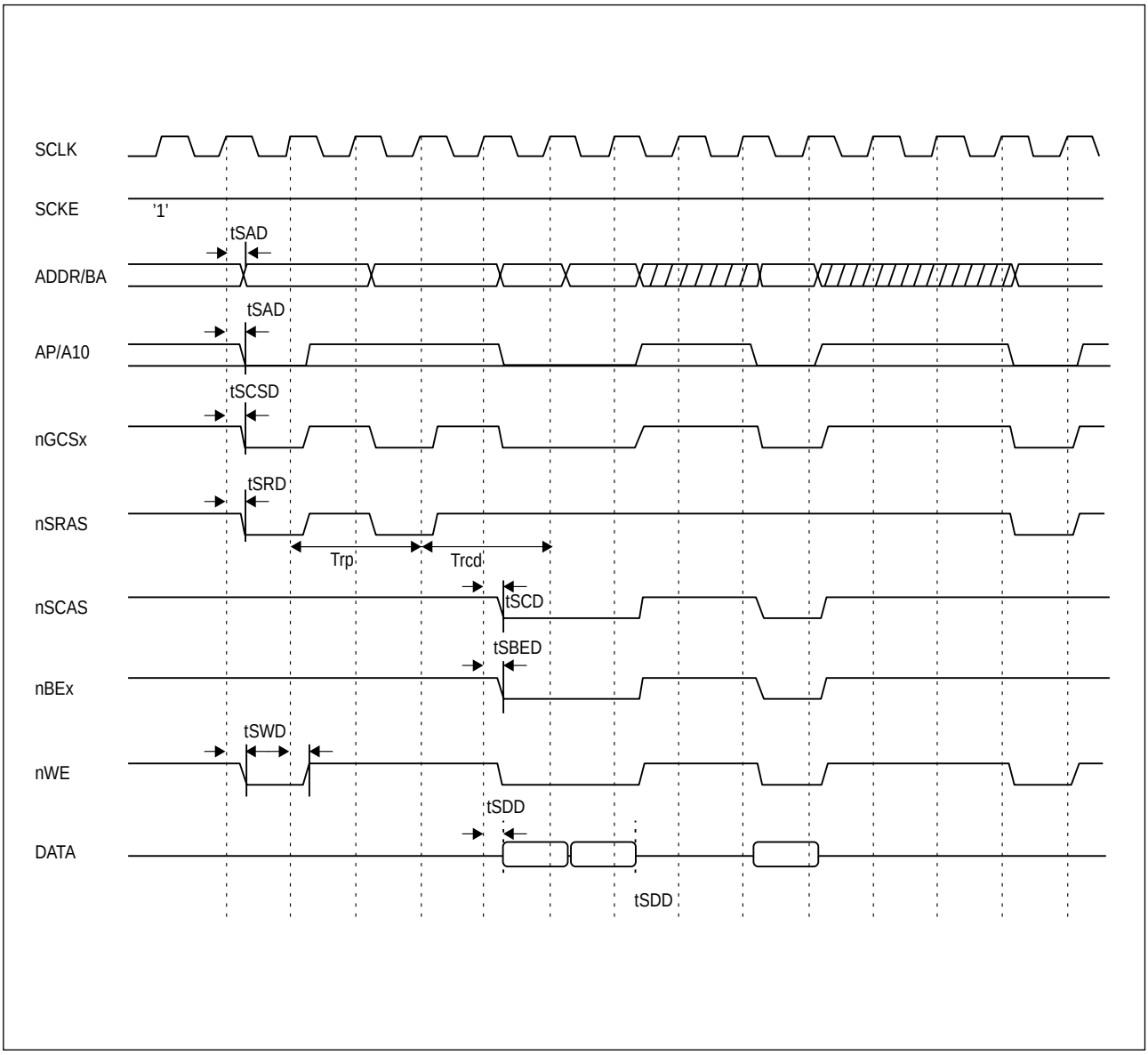

<Figure 6. SDRAM Write Timing>

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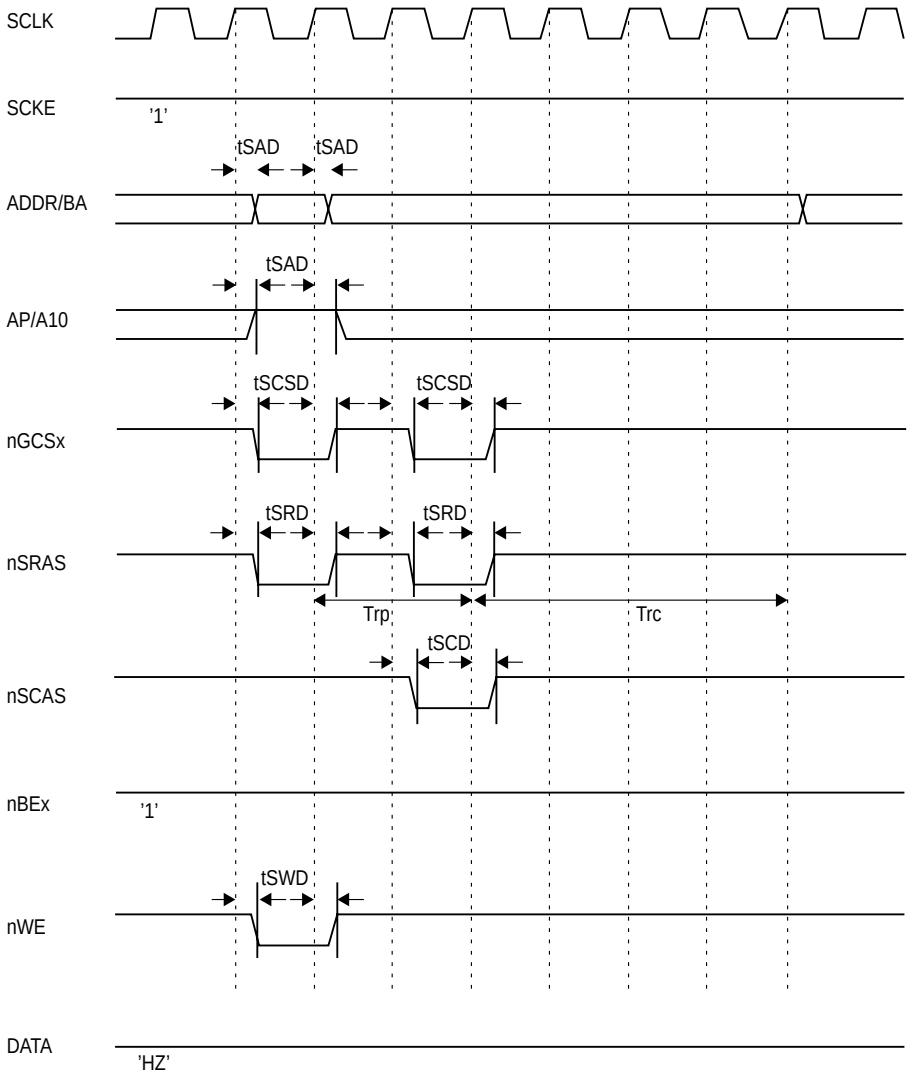

<Figure 7. SDRAM Write Timing>

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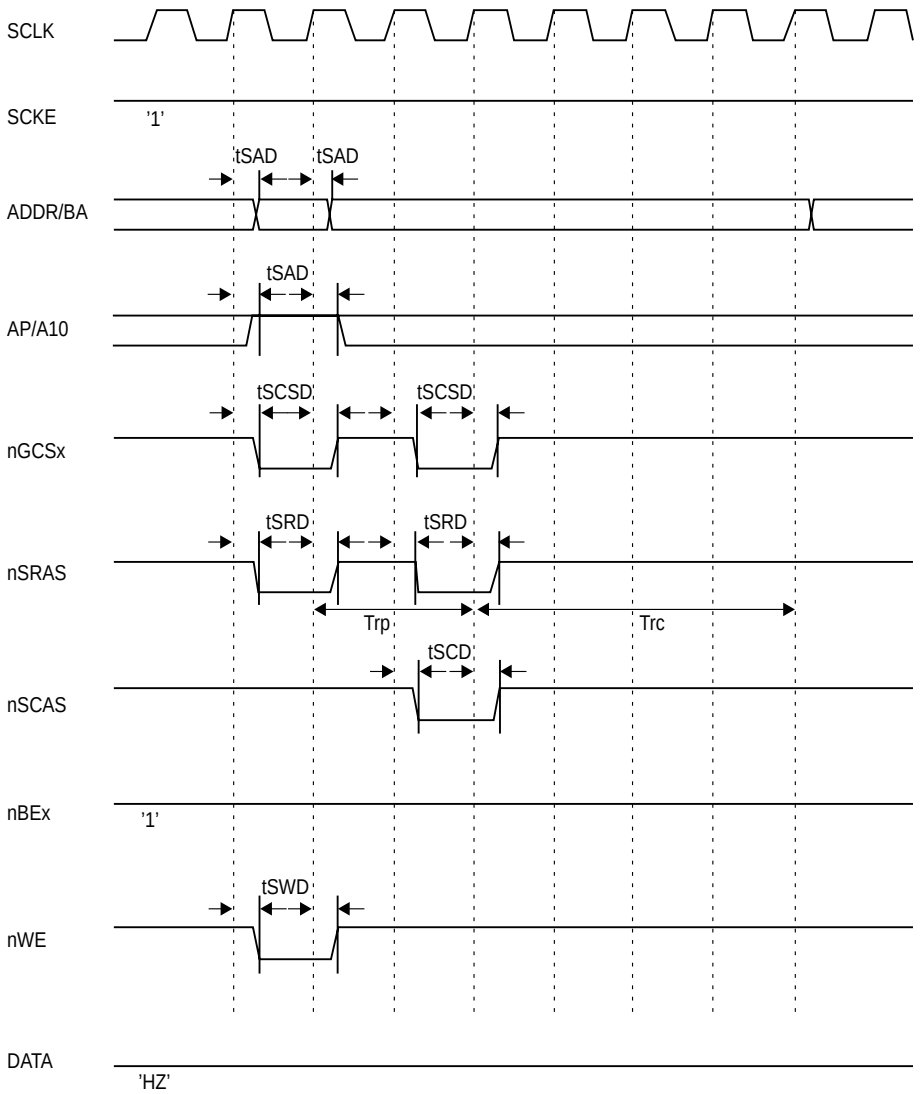

<Figure 8. SDRAM auto Refresh Timing>

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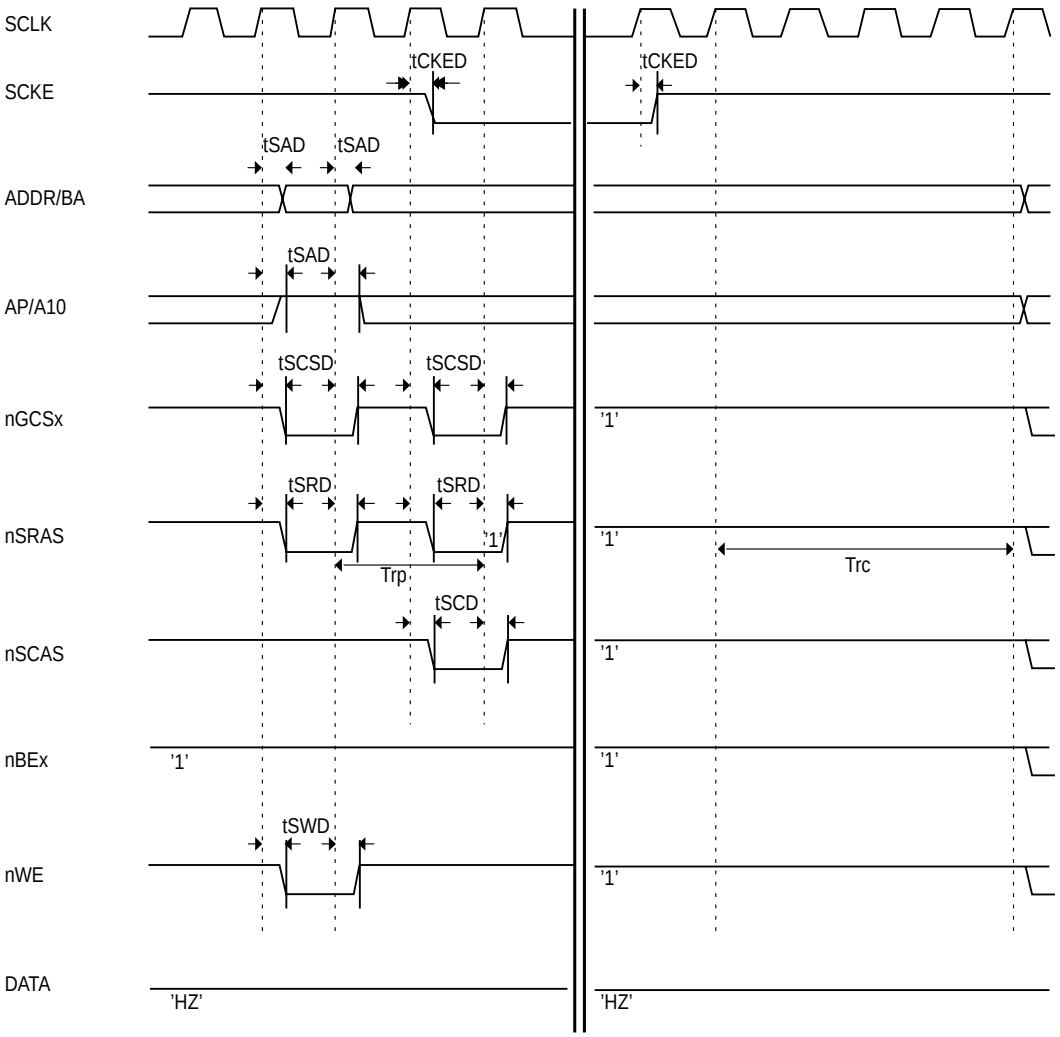

<Figure 9. SDRAM Self Refresh Timing>

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<3> EXTERNAL DMA part

This system does not use External DMA part.

<4> DRAM control part

Since S3C46Q0X has the DRAM CONTROLLER build-in, it may be used by connecting DRAM with external memory. The Control mode of DRAM CONTROLLER provided by S3C46Q0X is available for EARLY WRITE, NORMAL READ, PAGE MODE, and BYTE_HALF WORD ACCESS, and is supported even by EDO DRAM,and SDRAM as well as, Fast page DRAM. This system uses SDRAM, and the signal used for READ_WRITE uses _RD,_WR signal used for SYSTEM BUS CONTROL. It is supported with auto REFRESH and also by the Self-refresh mode for DRAM BACK UP. It consists of 2 Banks connected to common _SCSO, _SCAS, _SRAS, _SCLK, _SCKE, _DQM[1:0], each of them may use up to 2M ~ 32M HALF WORD.

In this system, Basic 2MB (TAD 8MB) is applied as system memory. The area of DRAM is specified in the DRAM MEMORY MAP of Fig. 1, while the related TIMING DIAGRAM in Fig. 5, 6, 7, 8, 9.

<5> RTC (REAL TIME CLOCK) part

S3C46Q0X real time clock (RTC) operates by the super capacitor although the system power turns off. In case of the Basic, the backup is operated with the primary battery (CR2032), and in case of the TAD, the backup is operated with the secondary battery (Super-cap). The RTC has the time data that is stored as the 8 bit BCD (binary coded decimal) format. The data include second, minute, hour, date, day, month, and year. The RTC unit works with an external 32.768 kHz crystal and also can perform the alarm function and round reset function.

<6> PARALLEL PORT INTERFACE division

This system does not use Parallel Port Interface Division.

<7> USB INTERFACE PART

1. USB function description

As the mode of implementing low cost express PC Interface, USB was applied. At USB, PC plays the role of route hub simultaneously by existing in the highest level as the host. That is, the device supporting each USB is connected centering on PC.

The device is available for Interface for the maximum of 127. USB cable is composed of total of a set of twisted pair and 2 power lines. The part for implementing USB function is included in S3C46Q0X.

For Interface of USB, pull-up of 15KΩ is interfaced to the data line of high level instruments, and, among data lines of lower level instruments, pull-up resistance of 1.5KΩ is interfaced to any one.

At this time, DP line is pulled up for Full Speed device, and, for Low Speed device, DMline is pulled up. For upper level instruments(Host, HUB) speed of device is classified interfaced to low level by detecting any one among DP and DM. If both lines are in the level of GND at the same time, device is judged that low device is not interfaced. In the transmission mode of USB, there are (1) Control transmission, (2) Interrupt transmission, (3) Bulk transmission, isochronous transmission. Control transmission is for Host to find out configuration information from USB device. This is conducted when device is interfaced. Interrupt transmission is used when small quantity of data is sent periodically. Interval value may be known from device in the case of initial setting. Bulk transmission is valid in case of trying to transmit data in large quantities or in case of transmitting them accurately.

Isochronous transmission should be assured of bandwidth, and is used when transmitting large quantities of information. Data in voice is used where delay is not allowed but small error is allowed. At USB coding mode and bit supping are being conducted. First, in case original data is 1, bit shall not change, and only when original data is 001, it shall be inverted. Only while data is 1, 1 and 0 shall be repeated. Also, in case 1, original data, is continued in 6 bit, 0 shall be inserted, Also, in the 1st phase of packet, data in the synchronized pattern shall be sent. About more detailed information regarding USB,

see http//:www.usb.org.

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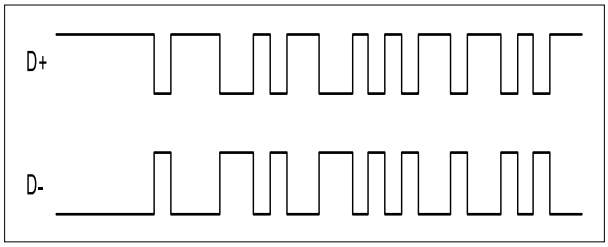
2. operation description

This system, when Host and USB cables are connected, and when +5V is detected in power detector inside chip and Vbus, 3.3V comes out through Pull-uP terminal. This is also connected to DP in pattern of hardware and supports Full-speed. Utilizing Configuration Endpoint, EPO, in USB controller, Plug & Play function is operated. Exchange of information between PCs is accomplished through DP and DM erminals. This terminal decides transmission speed depending on connection of regulator output in USB controller, and decides size of signal following USB and SPFC. Signal of general DP and DM terminals are same as Figure 10-3.

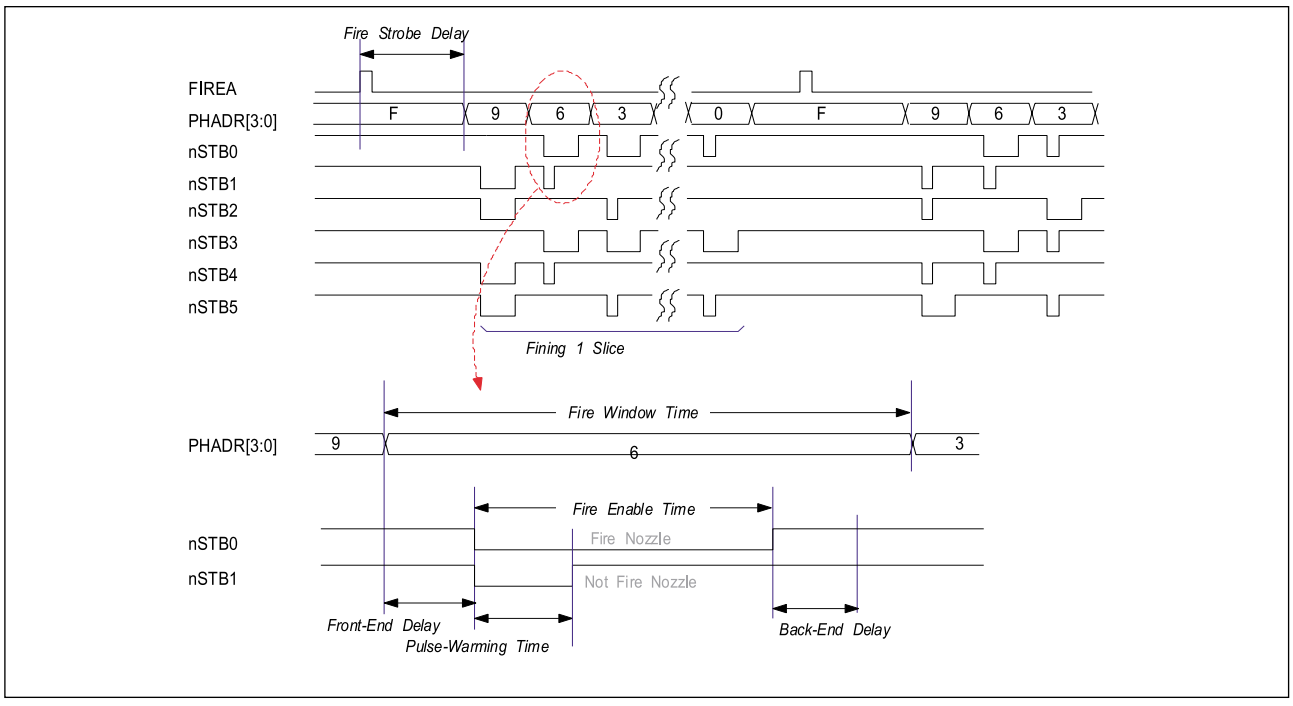


< Figure 10-3. USB Signal Line DIAGRAM >

<8> HEAD Control Part

1. General Information

It drives the Inkjet Head, and it controls the HA[3:0] and _STB[5:0], which control the Six-Shooter. The Six-shooter creates the signal to drive 48 Nozzle of the HEAD. The Stubby Head in the system is the Bubble type head, and has 48 nozzle for the Mono and Color(Printer only). 48 Nozzle Head of the mono and color head receives the data by 6 bytes per1 slice. The data from the HDMA goes to the CDE (Consecutive Dot Eliminator), DITH, and Data Out Block, and the data and address, controlled by the Fire signal and the Fire Window Time of the CRCON_CRFIRE Block, are outputted to the head Driver (Six-Shooter). The head consists of the 4 firing groups. Each group has 12~14 nozzles, and only one nozzle is firing per a Fire in each group. It means that one Fire can make 4 nozzles firing.



< Figure 12. Print48(HP) Firing Timing >

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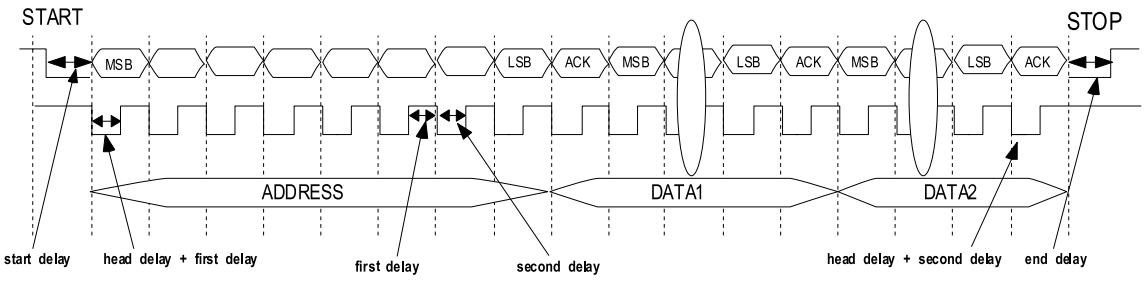
2. HEAD DATA OUTPUT FORMAT

The 1 slice data [47:0] from the HDMA is outputted with the PHADR in order as below.

nSTB0		nSTB1		nSTB2		nSTB3		nSTB4		nSTB5	
PHADR	DATA	PHADR	DATA	PHADR	DATA	PHADR	DATA	PHADR	DATA	PHADR	DATA
9	-	9	45	9	19	9	-	9	44	9	18
6	13	6	39	6	-	6	12	6	38	6	-
3	7	3	-	3	33	3	6	3	-	3	32
B	-	B	1	B	27	B	-	B	0	B	26
A	-	A	47	A	21	A	-	A	46	A	20
7	15	7	41	7	-	7	14	7	40	7	-
4	9	4	35	4	-	4	8	4	34	4	-
1	3	1	-	1	29	1	2	1	-	1	28
0	-	0	-	0	23	0	-	0	-	0	22
C	-	C	43	C	17	C	-	C	42	C	16
5	11	5	37	5	-	5	10	5	36	5	-
2	5	2	-	2	31	2	4	2	-	2	30
0	25	0	-	0	-	0	24	0	-	0	-

<9> SYNCHRONOUS SERIAL INTERFACE PART

It interfaces with Quarter-horse ASIC and consists of SMIC, SMID, PWM, and _RST. The Quarter-horse is the Motor Driver IC. The Quarter-horse interface Logic makes the data as a serial for transmitting the data to the Quarter-horse, and transmits the serial to the Quarter-horse IC by controlling it with the arranged Protocol. The Quarter-horse uses two signals, SMIC (clock) and SMID (data) to transmit the data. It transmits 3 bytes at once, and the 3 bytes mean the Device Address, Data 1, and Data 2. It is transmitted from MSB to LSB. The Quarter-horse sends the ACK signal at the end of the each byte to confirm the transmitted data. In case of no receiving ACK signal, the Quarter-horse_interface Logic sends the 3 bytes again. Depending on the level of the SMIC and SMID signals, the different messages are shown.



If it is high (SMIC) and high (SMID), it means the IDLE condition which means no data is received, if it is high (SMIC) and high-to-low-transition (SMID), it means the data transfer is started, and if it is high (SMIC) and low-to-high-transition (SMID), it means the last data transfer.

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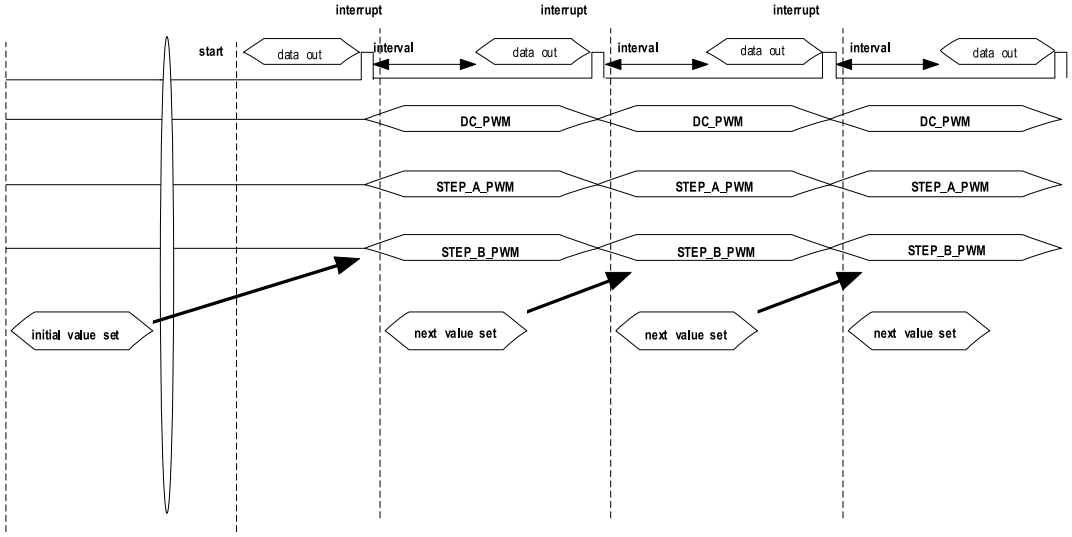

While transferring the motor phase, if there is NAK, the data transfer is automatically stopped and being in the IDLE condition. In the case, The S/W makes new value to transfer the data, or if the NAK Enable of the Control Register is set, automatically the same value is transferred for data transfer after for a while.Quarter-horse controls two Stepper motors (Line Feeder and Service Station) and one DC Motor (Carriage Motor).

<10> MOTOR Control Part

S3C46Q0X supports two Step Motors and one DC Motor, but only TX Scan Motor is used in the system. The Quarter-horse supports LF, SS, and CR MOTOR.

<11> S3C46QOX General Purpose I/O Port.

1. 1 Chorus-2 Assigned GCS Ports for RHINE

PORT NAME	PIN NO	I/O (Default)	SIGNAL NAME	DESCRIPTION	
				H	L
nGCS0	196	O	/ROM_CS	BASIC/TAD : FLASH MEMORY(8Mb) CHIP SELECT	
nGCS1/GPO16	198	O(H)	/MCS	MODEM CHIP SELECT	
nGCS2/GPO17	199	O(H)	/EN_PRN	SIXSHOOTER CHIP SELECT	
nGCS3/GPO18	200	O(H)	/SEL_COLOR	COLOR HEAD SELECT for ENERGY LEVEL CTL	
nGCS4/GPO19	201	O(H)	RX_CTL	REMOTE	RX LINE SIGNAL
nGCS5/GPO15/PDE	202	O(H)	TX_CTL	TX LINE SIGNAL	H/S MIC SIGNAL
nGCS6/nRAS0/nSCS0 /GPO13	46	O(H)	/SCS0	BASIC : SDRAM0(16Mb) CHIP SELECT TAD : SDRAM0(64Mb) CHIP SELECT or EMULATOR for J-TECH	
nGCS7/nRAS1/nSCS1 /GPO14	47	O(H)	EN_RTEST	HEAD RESISTOR TEST ON	IDLE

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2. Chorus-2 Assigned GPO Ports for RHINE

PORT NAME	PIN NO	I/O (Default)	SIGNAL NAME	DESCRIPTION	
				H	L
GPO0/nRESET_OUT	94	O(H)	_F_POR	WATCHDOG RESET OFF (Watchdog Reset Out & FLASH RESET OUT)	WATCHDOG RESET ON
GPO1/TONE_OUT	102	O(L)	KEY CLICK	KEY CLICK	
GPO2/nFAULT	116	O(H)	TONE_CTL	KEY CLICK	LINE MONITORING
GPO3/PERROR	118	O(L)	_MODEM_RST	MODEM RESET OUT	
GPO4/SELECT	117	O(L)	CML_CTL1	CML_CTL1 ON	CML_CTL1 OFF
GPO5/nACK	120	O(H)	HS_VOL_CTL	USA(Only) VOLUME UP	IDLE
GPO6/BUSY	119	O(H)	_SPK_CTL	AUDIO AMP OFF	AUDIO AMP ON
GPO7/TXD0	64	O(H)	OPE_TXD	UART TXD for OPE	
GPO8/PLOAD/PHADDR1	128	O(H)	HA1	ADDR1 for HP HEAD DRIVER (PHADDR0/1/2/3)	
GPO9/XnDACK0	68	O(H)	CML_CTL2	CML_CTL2 ON or (LT)	CML_CTL2 OFF or (LT)
GPO10/SCKE	50	O(H)	SD_CKE	SDRAM CLOCK ENABLE	
GPO11 /nBE0/nWE0/DQM0	51	O(H)	DQM0	SDRAM0 MASK SIGNAL	
GPO12 /nBE1/nWE1/DQM1	52	O(H)	DQM1	SDRAM1 MASK SIGNAL	
GPO13 /nGCS6/nRAS0/nSCS0	46	O(H)	_SCS0	BASIC : SDRAM0(16Mb) CHIP SELECT TAD : SDRAM0(64Mb) CHIP SELECT or EMULATOR for J-TECH	
GPO14 /nGCS7/nRAS1/nSCS1	47	O(H)	EN_RTEST	HEAD RESISTOR TEST ON	IDLE
GPO15/nGCS5/PDE	202	O(H)	TX_CTL	TX LINE SIGNAL	H/S MIC SIGNAL
GPO16/nGCS1	198	O(H)	_MCS	MODEM CHIP SELECT	
GPO17/nGCS2	199	O(H)	_EN_PRN	SIXSHOOTER CHIP SELECT	
GPO18/nGCS3	200	O(H)	_SEL_COLOR	COLOR HEAD SELECT for ENERGY LEVEL CTL	
GPO19/nGCS4	201	O(H)	RX_CTL	RX LINE SIGNAL	REMOTE
GPO20/nCAS0/nSCAS /TPH_STB2	44	O(H)	_SD_CAS	SDRAM0 COLUMN ADDRESS STROBE	
GPO21/nCAS1/nSRAS /TPH_STB3	45	O(H)	_SD_RAS	SDRAM0 ROW ADDRESS STROBE	
GPO22/ADDR22	41	O(L)	A22	64Mb SDRAM BA1 SIGNAL	
GPO23/ADDR23	42	O(L)	_OPE_RST	OPE RESET OUT	
GPO24/ADDR24	43	O(L)	B_TSR_ON	BLACK HEAD TEST ON	IDLE

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3. Chorus-2 Assigned GPI Ports for RHINE

PORT NAME	PIN NO	I/O	SIGNAL NAME	DESCRIPTION	
				H	L
GPI0/TMS	54	I	TMS	TMS for JTAG	
GPI1/nAUTOFD	115	I	_HOOK_DET1	HANDSET HOOK ON	HANDSET HOOK OFF
GPI2/nSLCTIN	112	I	_HOOK_DET2	EXT. PHONE HOOK ON	EXT. PHONE HOOK OFF
GPI3/nINIT	114	I	_RING_DET	IDLE	RING DETECTED
GPI4/nSTROBE	113	I	_SS_SW	IDLE	SS_SWITCH ON
GPI5/RXD1/SIOCLK1	67	I	-	RESERVED	
GPI6/RXD0	65	I	OPE_RXD	UART RXD for OPE	
GPI7/CRY/LFPHA_IA0	84	I	_P_PICKUP	IDLE I PAPER DETECTED P_EXIT SENSOR INPUT	
GPI8/CRX/LFPHA_IA1	83	I	TEMPOUT	TEMP. DATA INPUT for TEMP IC	
GPI9/LSU_nFSYNC /CHY/CRPHA_IA0	77	I	CHY	CHX for HP CR ENCODER	
GPI10/PVC_nHSYNC /CHX/CRPHA_IA1	76	I	CHX	CHY for HP CR ENCODER	
GPI11/XnDREQ0	69	I	-	RESERVED (H/W PULL-UP)	
GPI12/XnDREQ1	71	I	-	RESERVED (H/W PULL-UP)	
GPI13/EINT0	193	I	_MIRQ	MODEM INTERRUPT INACTIVE I MODEM INTERRUPT ACTIVE /MODEM_IRQ2 INPUT	
GPI14/EINT1	194	I	HEAD_ID	HEAD ID DATA INPUT	
GPI15/EINT2	195	I	RTEST	HEAD REGISTER TEST DATA INPUT	
GPI16/XnWAIT	93	I	-	RESERVED (H/W PULL-UP)	

4. Chorus-2 Assigned GPIO Ports for RHINE

PORT NAME	PIN NO	I/O	SIGNAL NAME	DESCRIPTION	
				H	L
GPIO0/ADC_DATA0 /DONE_BIST1	182	O(B)	HS_TX_CTL	HANDSET TX ON	HANDSET TX OFF (IDLE)
GPIO1/ADC_DATA1 /DONE_BIST2	183	O(B)	HS_RX_CTL	HANDSET RX ON	HANDSET RX OFF (IDLE)
GPIO2/ADC_DATA2 /DIAG_BIST1	184	O(B)	DP	DP DIAL(RECALL) PULSE ON	DP DIAL(RECALL) PULSE OFF
GPIO3/ADC_DATA3 /DIAG_BIST2	185	O(B)	-	RESERVED	
GPIO4/ADC_DATA4 /ERRORB_BIST1	186	O(B)	-	RESERVED	
GPIO5/ADC_DATA5 /ERRORB_BIST2	187	O(B)	-	RESERVED	
GPIO6/ADC_DATA6	188	O(B)	V0L_A	VOL_C VOL_B VOL_A 14051 MUX SELECT H H H VOLUME 7 : RING VOLUME MAX H H L VOLUME 6 : RING VOLUME H L H VOLUME 5 : RING VOLUME H L L VOLUME 4 : RING VOLUME MIN L H H VOLUME 3 : LINE MONITORING VOL MAX L H L VOLUME 2 : LINE MONITORING VOL L L H VOLUME 1 : LINE MONITORING VOL L L L VOLUME 0 : LINE MONITORING VOL MIN	
GPIO7/ADC_DATA7	190	O(B)	VOL_B		
GPIO8/ADC_DATA8	191	O(B)	VOL_C		
GPIO9/ADC_DATA9	192	B	-	RESERVED	

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5. HP IMPORTANT ASIC Ports for RHINE

PORT NAME	PIN NO	CPU I/O	SIGNAL NAME	DESCRIPTION	
				H	L
ERTE ASIC					
B_TSR_ON	68	O	B_TSR_ON	BLACK HEAD TEST ON	
EN_RTEST	47	O	EN_RTEST	HEAD REGISTER TEST ENABLE	
TEMPOUT	83	I	TEMPOUT	TEMP. OUTPUT	
HEAD_ID	194	I	HEAD_ID	HEAD ID OUTPUT	
RTEST	195	I	RTEST	HEAD REGISTER TEST OUTPUT/ID OUTPUT	
PWM_OFFSET	80	O	PWM_OFFSET	B_TSR OFFSET	
PWM_REF	81	O	PWM_REF	TEMP. REFERENCE	
QUARTER HORSE					
SMIC	72	O	SMIC	SERIAL MOTOR INTERFACE CLOCK for Q.H	
SMID	101	B	SMID	SERIAL MOTOR INTERFACE DATA for Q.H	
PWM_PS	79	O	PWM_PS	POWER SUPPLY PWM for 19.2V CALIBRATION for Q.H	
CMPWM	78	O	CMPWM	CARRIAGE MOTOR PWM for Q.H	
SPWMA	86	O	SPWMA	STEP MOTOR PHASE A,/A CURRENT CTL for Q.H	
SPWMB	85	O	SPWMB	STEP MOTOR PHASE B,/B CURRENT CTL for Q.H	
SIX SHOOTER					
SEL_COLOR	200	O	SEL_COLOR	COLOR HEAD SELECT for ENERGY LEVEL CTL	
EN_PRN	199	O	_EN_PRN	SIXSHOOTER CHIP SELECT	
HA3	121	O	HA3	HEAD DRIVER ADDRESS(3:0) for HP HEAD	
HA2	95	O	HA2		
HA1	128	O	HA1		
HA0	127	O	HA0		
nSTB5	96	O	_STB5	HEAD SELECT(5:0) for HP HEAD	
nSTB4	97	O	_STB4		
nSTB3	123	O	_STB3		
nSTB2	124	O	_STB2		
nSTB1	125	O	_STB1		
nSTB0	126	O	_STB0		
SENSOR					
CHX	76	I	CHX	CHX for HP CR ENCODER	
CHY	77	I	CHY	CHY for HP CR ENCODER	
_SS_SW	113	I	SS_SW	SERVICE STATION MOTOR INPUT	

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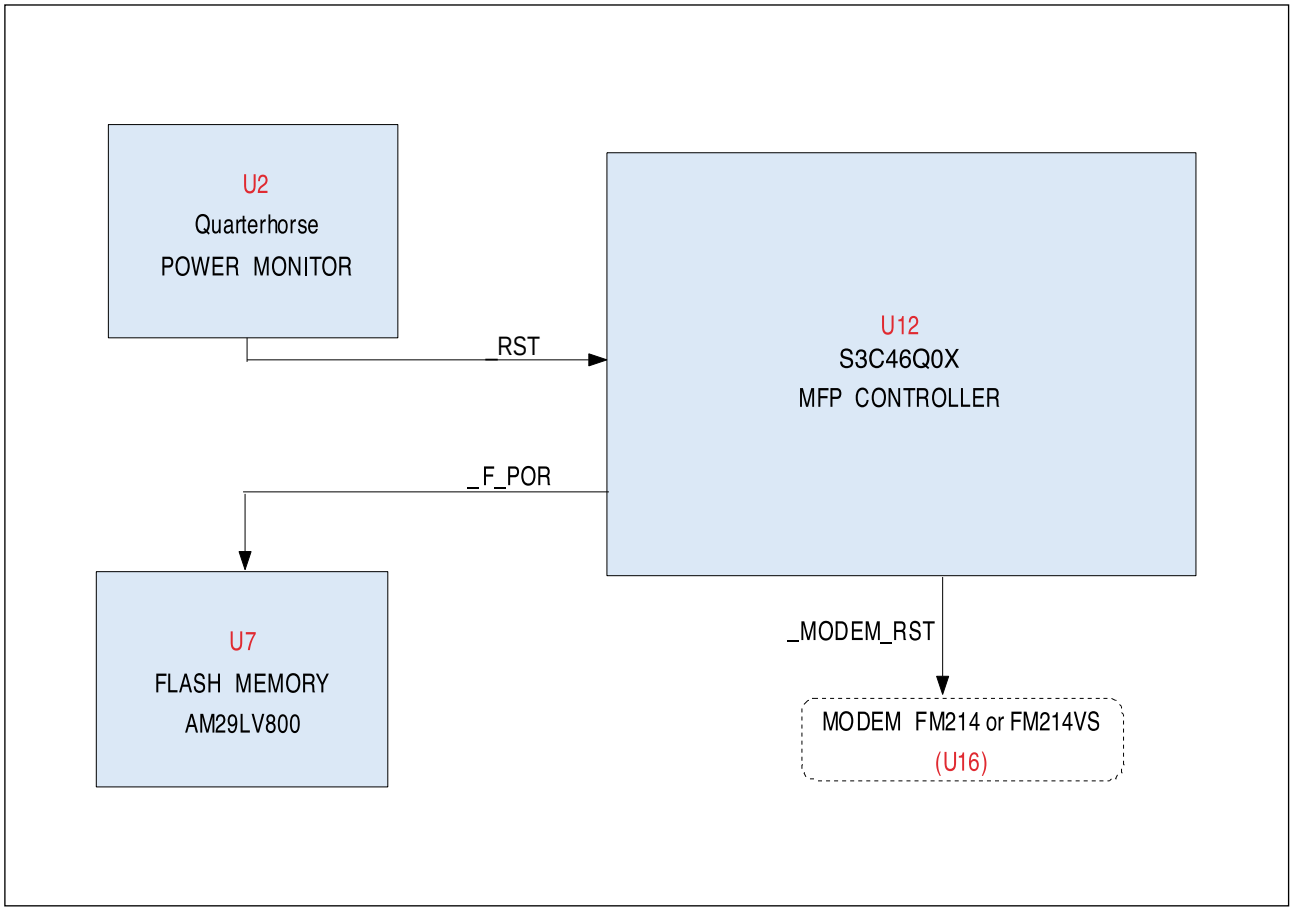
3.1.3.3 RESET circuit

This system is configured with PRIMARY RESET(_RST) of Power Reset, Reset by WATCH DOG TIMER, external PRIMARY RESET, and SECOND RESET(__F_POR) which was done AND. PRIMARY RESET SYSTEM is used for resetting MAIN CONTROLLER(U12) when System Power is authorized, and SECOND RESET resets FLASH MEMORY(U7). Figure below is BLOCK DIAGRAM related to the reset of entire system.

When +5V reaches +4.75V so that system may operate, POWER MONITOR(U2) moves to High(+5V) after maintaining low(OV) in the degree of 50mS-200mS output while monitoring it. This Reset signal is input into MFP CONTROLLER(S3C46Q0X, U12) right away, and MFP CONTROLLER becomes awake. And it releases _F_POR after MCLK 1 clock. The Quarter-horse needs +24V to be operated, but +5.0V is supplied by the Buck Regulator circuit. If +5.0V is incompletely supplied such as +4.75V, it is checked as the Power Failure. The _RST output becomes low (0V), and the S3C46Q0X (U12) confirms it to make it RESET (LOW ACTIVE). When the S3C46Q0X is released from RESET, the _F_POR of the S3C46Q0X and FLASH MEMORY are reset.

<1> WATCH DOG OUTPUT (_F_POR)

Since WATCH DOG TIMER, which is Programmable Counter in (S3C46Q0X, U12) is set as disable for INITIAL STATE, it shall be set as Disable so that it won't operate, and after it is initialized for operation, it shall be reused by setting it Enable. When Watch Dog Reset occurs, it is about 10mS depending on the value set at the initial stage. And Counter value of Watch Dog Timer is changed by the program. Reset signal (_F_POR,U12-94) shall be generated, and entire system shall be Reset and initialized.



< Figure 13. POWER RESET BLOCK DIAGRAM >

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3.1.4 MEMORY

3.1.4.1 General description

MEMORY applied in this system are FLASH MEMORY(U7) of 1Mbyte, SDRAM (SF-330/331P:U9 ; 2Mbyte ,/ SF-335T : U8 ; 8Mbyte)

3.1.4.2 MEMORY configuration

By each CHIP SELECT (ROM_CS, _SCS0, _SD_RAS ,_SD_CAS), FLASH MEMORY and SDRAM are selected, and DATA is accessed by HALF WORD unit.

3.1.5 Image Processing Part

3.1.5.1 General description

The image processor, built-in to Chorus-2 is consisted of Scanner Interface, Motor control, Shading Acquisition _ Shading Correction, Gamma Correction, Vertical Decimation, Horizontal Enlargement/Decimation and Binarization. (See Figure 16)

3.1.5.2 Features & Functions

- 0.18µm CMOS process, 208-pin QFP, std 130 library
- Frequency : 66MHz(15ns)
- Image Sensor I/F : 200/300/600dpi CIS or CCD
- Scanning Function
  - Color Gray Image : each 8 bits / RGB
  - Mono Gray Image : 8 bits / pixel
- Maximum processing Width
  - A4, 600 dpi
  - 5KB Effective pixel
- Ideal MSLT (Minimum Scan Line Time)
  - Grey mode(Color) : 3(RGB) X 5KB X 15nsec X 16clock =3.69 msec
  - Grey mode(mono) : 1 X 5KB X 15nsec X 16clock =1.23 msec
  - Grey mode(Color) : 1 X 5KB X 15nsec X 16clock =1.23 msec
- A/D conversion depth : 10 bits

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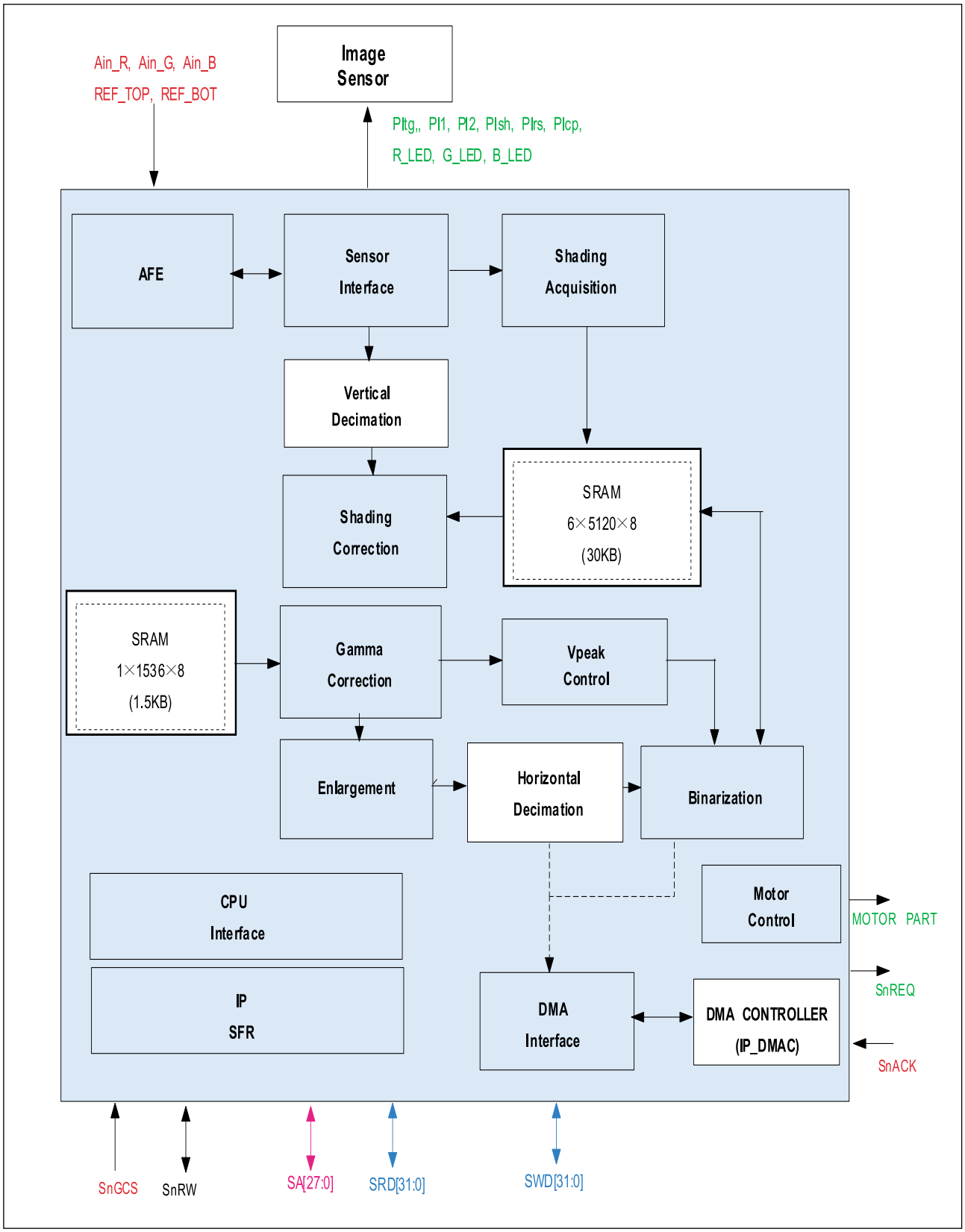
3.1.5.3 Block Diagram



<Figure 16. Block Diagram of IP_TOP>

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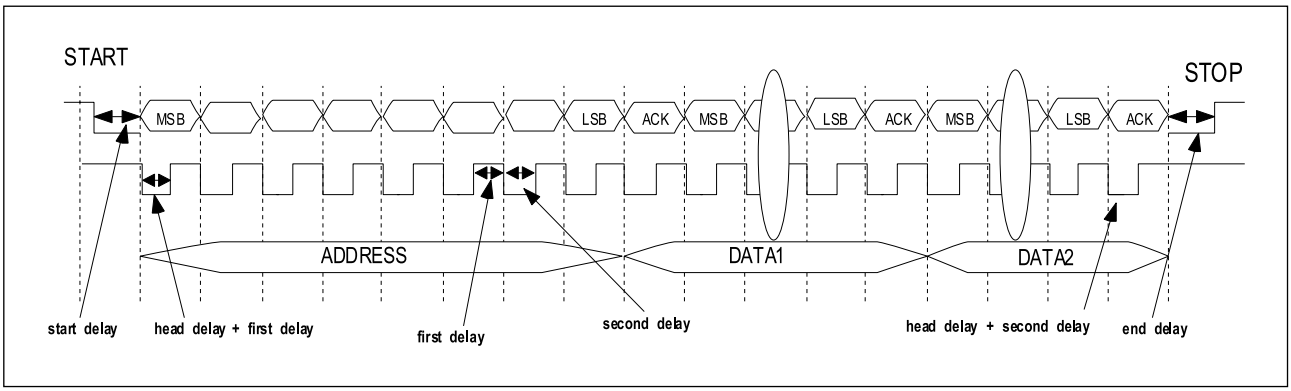
3.1.6 QUARTERHORSE ASIC

3.1.6.1 General Information

The Quarter-horse ASIC consists of the Serial Interface port which interfaces with the main controller, Linear Pre-regulator Circuit, Power On Reset Generation Circuit, and Motor Drive part.

<1> SERIAL INTERFACE

It interfaces with the Main Controller (S3C46Q0X), and consists of SMIC, SMID, PWM, and _RST. Please, refer to the picture 17 for the timing.



< Figure 17. SERIAL INTERFACE INPUT timing diagram>

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<2> SERIAL INTERFACE

PIN NAME	DESCRIPTION	DIRECTION / TYPE
preg	Pre-regulator control	analog/output
Vin	DC motor driver and 5V regulator input supply voltage	power/input
DCMA	DC motor drive half bridge A	power/bidirectional
DCMB	DC motor drive half bridge B	power/bidirectional
DCPWM	PWM input signal	CMOS/input
nPA	Paper motor phase A drive	power/open drain
nPnA	Paper motor phase nA drive	power/open-drain
nPB	Paper motor phase B drive	power/open drain
nPnB	Paper motor phase nB drive	power/open drain
+12V	+12V EEPROM programming voltage	output
nSA	Service station motor phase A drive	power/open drain
nSnA	Service station motor phase nA drive	power/open drain
nSB	Service station motor phase B drive	power/open drain
nSnB	Service station motor phase nB drive	power/open drain
DATA	Serial Data Input (and ACK output)	CMOS/input
SCLK	Serial Clock Input	CMOS/input
GATE1	V1 gate drive	power/output
SOURCE1	V1 source voltage return	analog/input
Vfb	V1 return to close loop	analog/input
COMP1	V1 compensation pin	analog
SWITCH	+5V switching output	power/output
COMP5	+5V compensation pin	analog
+5V	+5V input for logic and to close loop	analog/input
Vdd	Input Voltage	power/input
CP1	Bootstrap capacitor pin 1	analog
CP2	Bootstrap capacitor pin 2	analog
Ground	Ground	analog
nRESET	Active low totem pole reset output	CMOS/output
Enable	Chip Enable	CMOS/input
CT	Reset timing delay capacitor	analog
SPWMA	Stepper motor pwm phase A/nA	CMOS/input
SPWMB	Stepper motor pwm phase B/nB	CMOS/input
Vp	Boost voltage output for high side FETs	power/output
GND (11)	Used both as ground and as heatsinking	analog

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3.1.6.2 QUARTERHORSE FUNCTION

<1> PEN / MOTOR SUPPLY VOLTAGE REGULATOR

It receives the inputted power of +24V, and the power flows to the buck type regulator, which consists of the external N-channel FET and SCHOTTKY diode, to make +19.2V. The power uses as the main power of the ink head, CR, and LF, SS MOTOR.

<2> +5V REGULATOR

The +24V (inputted power) is supplied, and it becomes +5V of the logic power by using the internal switching FET Buck type regulator. It becomes +3.3V to support the main power of the CPU by using external +3.3V Regulator, and the +3.3V becomes +1.8V to support the internal power of the CPU by using +1.8 Regulator.

<3> RESET CIRCUIT

The Reset of the Quarter-horse starts to work when the +5V is going down under +4.75V. It has the 1.5~5 usec of Sensitivity Timing Margin for preventing the minute shakiness of the power by ESD. Also, the Time Delay of the Reset can be controlled from 1ms to 1s by the Capacitor when power on.

<4> MOTOR DRIVERS

The Quarter-horse drives one DC Motor and two stepping motors. The DC Motor drives +19.2V as the FULL H-BRIDGE, and the direction information goes to the CPU via the Serial Interface port. Also, it is inputted the PWM Modulator from CPU. The Stepping Motor is driven by the UNIPOLAR, and the phase information is transmitted to the CPU via the Serial Interface port.

1. DC MOTOR TRUTH TABLE

DCA	DCB	PWM	A high side	A low side	B high side	B low side
0	0	X	off	on	off	on
0	1	0	on	off	on	off
0	1	1	off	on	on	off
1	0	0	on	off	on	off
1	0	1	on	off	off	on
1	1	X	on	off	on	off

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2. STEPPER MOTOR TRUTH TABLES

<PAPER MOTOR>

Inputs			Outputs		
Whinny Register Bits			Pin 38 (37)	Pin 35(31)	Pin 33(29)
PPWM	**pa (pb)**	**pna (pnb)**	**SPWMA (SPWMB)**	**nPA (nPB)**	**nPnA (nPnB)**
0	0	0	0	off	off
0	0	0	1	off	off
0	0	1	0	off	on
0	0	1	1	off	on
0	1	0	0	on	off
0	1	0	1	on	off
0	1	1	0	off	off
0	1	1	1	off	off
1	0	0	0	off	off
1	0	0	1	off	off
1	0	1	0	on	off
1	0	1	1	off	on
1	1	0	0	off	on
1	1	0	1	on	off
1	1	1	0	off	off
1	1	1	1	off	off

<SERVICE STATION MOTOR>

Inputs			Outputs		
Whinny Register Bits			Pin 38 (37)	Pin 36(32)	Pin 34(30)
PPWM	sa (sb)	sna (snb)	SPWMA (SPWMB)	nSA (nSB)	nSnA (nSnB)
0	0	0	0	off	off
0	0	0	1	off	off
0	0	1	0	on	off
0	0	1	1	off	on
0	1	0	0	off	on
0	1	0	1	on	off
0	1	1	0	off	off
0	1	1	1	off	off
1	0	0	0	off	off
1	0	0	1	off	off
1	0	1	0	off	on
1	0	1	1	off	on
1	1	0	0	on	off
1	1	0	1	on	off
1	1	1	0	off	off
1	1	1	1	off	off

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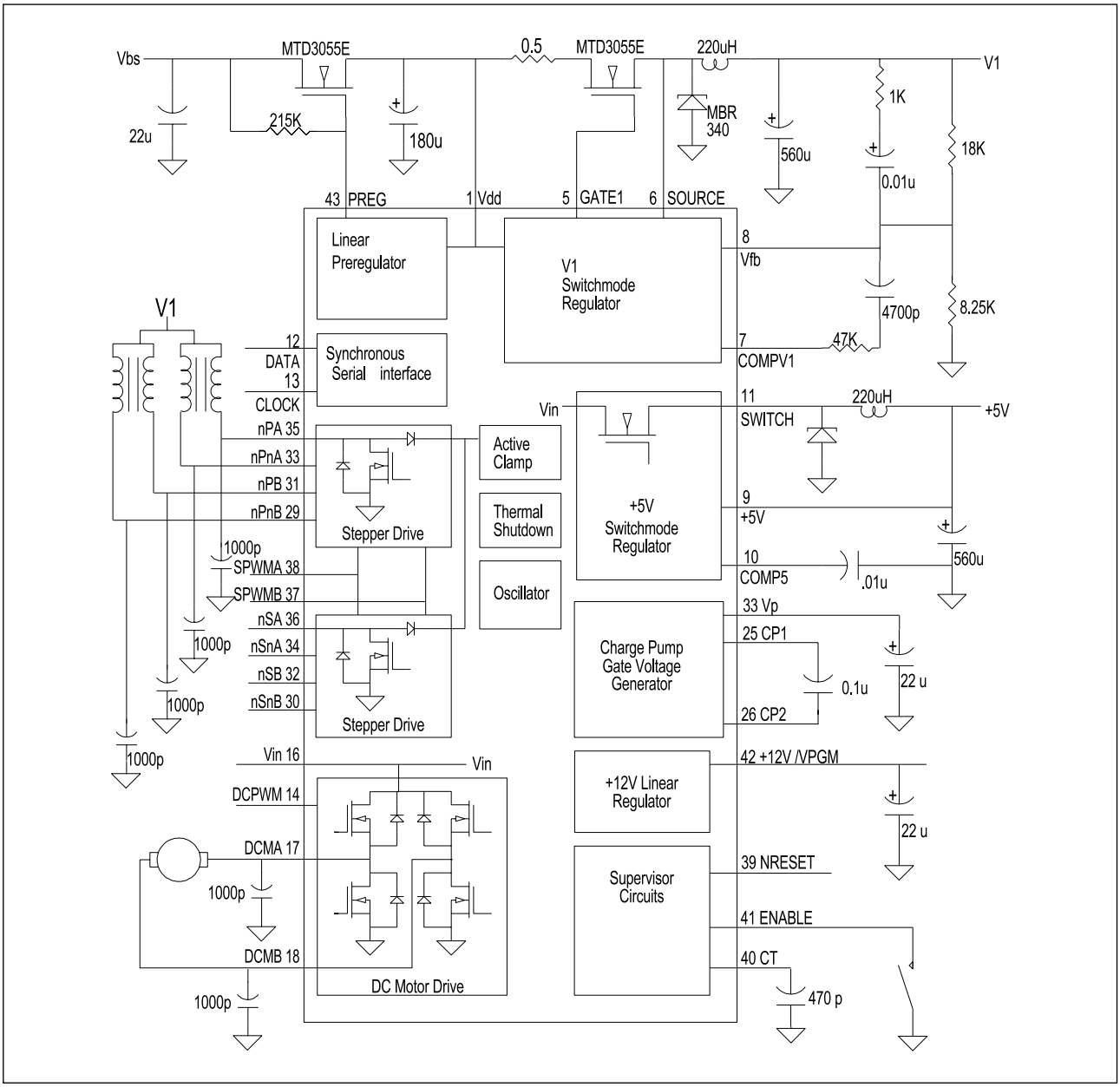
<5> Quarterhorse Block Diagram



<Figure 18. Quarterhorse Block Diagram showing typical external components>

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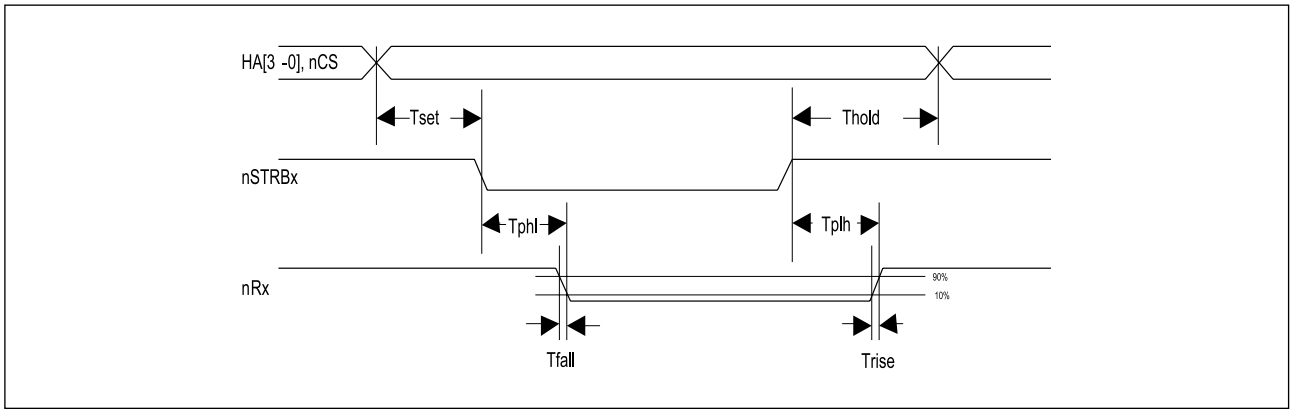
3.1.6 SIXSHOOTOR ASIC

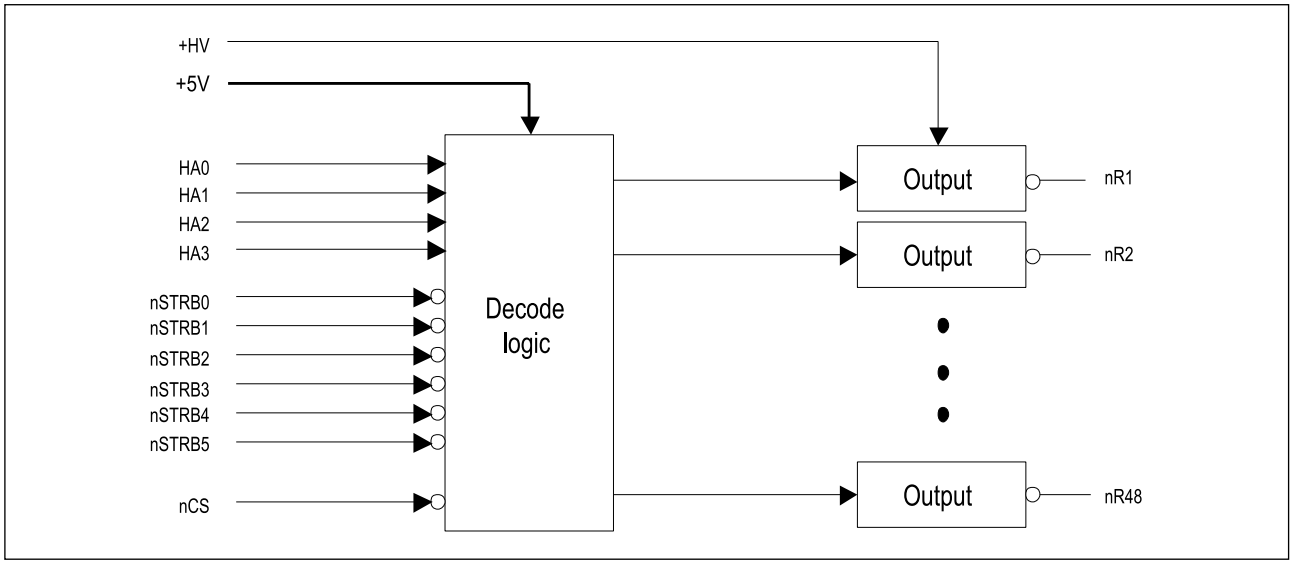
3.1.6.1 General Information

The Six-shooter ASIC exists for operating the Ballast Resistor and TIJ 2.0 Inkjet Head, and it has 4 head address HA [3-0], input of the 6 strobe nSTB [5-0], and output of the 48 nozzle control.

3.1.6.2 OPERATE TIMING AND INTERNAL BLOCK DIAGRAM



<figure 19. SIXSHOOTER Power Driver Driver Diagram>



<figure 20. SIXSHOOTER inside Block diagram>

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3.1.6.3 Decoder Logic Truth Table

nCS	HA3	HA2	HA1	HA0	nSTRB5	nSTRB4	nSTRB3	nSTRB2	nSTRB1	nSTRB0	nRx
1	X	X	X	X	X	X	X	X	X	X	None
0	X	X	X	X	1	1	1	1	1	1	None
0	X	0	0	0	X	X	X	X	X	0	R26
0	X	0	0	1	X	X	X	X	X	0	R4
0	X	0	1	0	X	X	X	X	X	0	R6
0	X	0	1	1	X	X	X	X	X	0	R8
0	X	1	0	0	X	X	X	X	X	0	R10
0	X	1	0	1	X	X	X	X	X	0	R12
0	X	1	1	0	X	X	X	X	X	0	R14
0	X	1	1	1	X	X	X	X	X	0	R16
0	0	X	0	0	X	X	X	X	0	X	R36
0	0	X	0	1	X	X	X	X	0	X	R38
0	0	X	1	0	X	X	X	X	0	X	R40
0	0	X	1	1	X	X	X	X	0	X	R42
0	1	X	0	0	X	X	X	X	0	X	R44
0	1	X	0	1	X	X	X	X	0	X	R46
0	1	X	1	0	X	X	X	X	0	X	R48
0	1	X	1	1	X	X	X	X	0	X	R2
0	0	X	0	0	X	X	X	0	X	X	R24
0	0	X	0	1	X	X	X	0	X	X	R30
0	0	X	1	0	X	X	X	0	X	X	R32
0	0	X	1	1	X	X	X	0	X	X	R34
0	1	X	0	0	X	X	X	0	X	X	R18
0	1	X	0	1	X	X	X	0	X	X	R20
0	1	X	1	0	X	X	X	0	X	X	R22
0	1	X	1	1	X	X	X	0	X	X	R28
0	X	0	0	0	X	X	0	X	X	X	R25
0	X	0	0	1	X	X	0	X	X	X	R3
0	X	0	1	0	X	X	0	X	X	X	R5
0	X	0	1	1	X	X	0	X	X	X	R7
0	X	1	0	0	X	X	0	X	X	X	R9
0	X	1	0	1	X	X	0	X	X	X	R11
0	X	1	1	0	X	X	0	X	X	X	R13
0	X	1	1	1	X	X	0	X	X	X	R15
0	0	X	0	0	X	0	X	X	X	X	R35
0	0	X	0	1	X	0	X	X	X	X	R37
0	0	X	1	0	X	0	X	X	X	X	R39
0	0	X	1	1	X	0	X	X	X	X	R41
0	1	X	0	0	X	0	X	X	X	X	R43
0	1	X	0	1	X	0	X	X	X	X	R45
0	1	X	1	0	X	0	X	X	X	X	R47
0	1	X	1	1	X	0	X	X	X	X	R1
0	1	X	1	1	0	X	X	X	X	X	R27
0	0	X	1	1	0	X	X	X	X	X	R33
0	1	X	0	1	0	X	X	X	X	X	R19
0	0	X	0	1	0	X	X	X	X	X	R29
0	1	X	1	0	0	X	X	X	X	X	R21
0	0	X	1	0	0	X	X	X	X	X	R31
0	1	X	0	0	0	X	X	X	X	X	R17
0	0	X	0	0	0	X	X	X	X	X	R23

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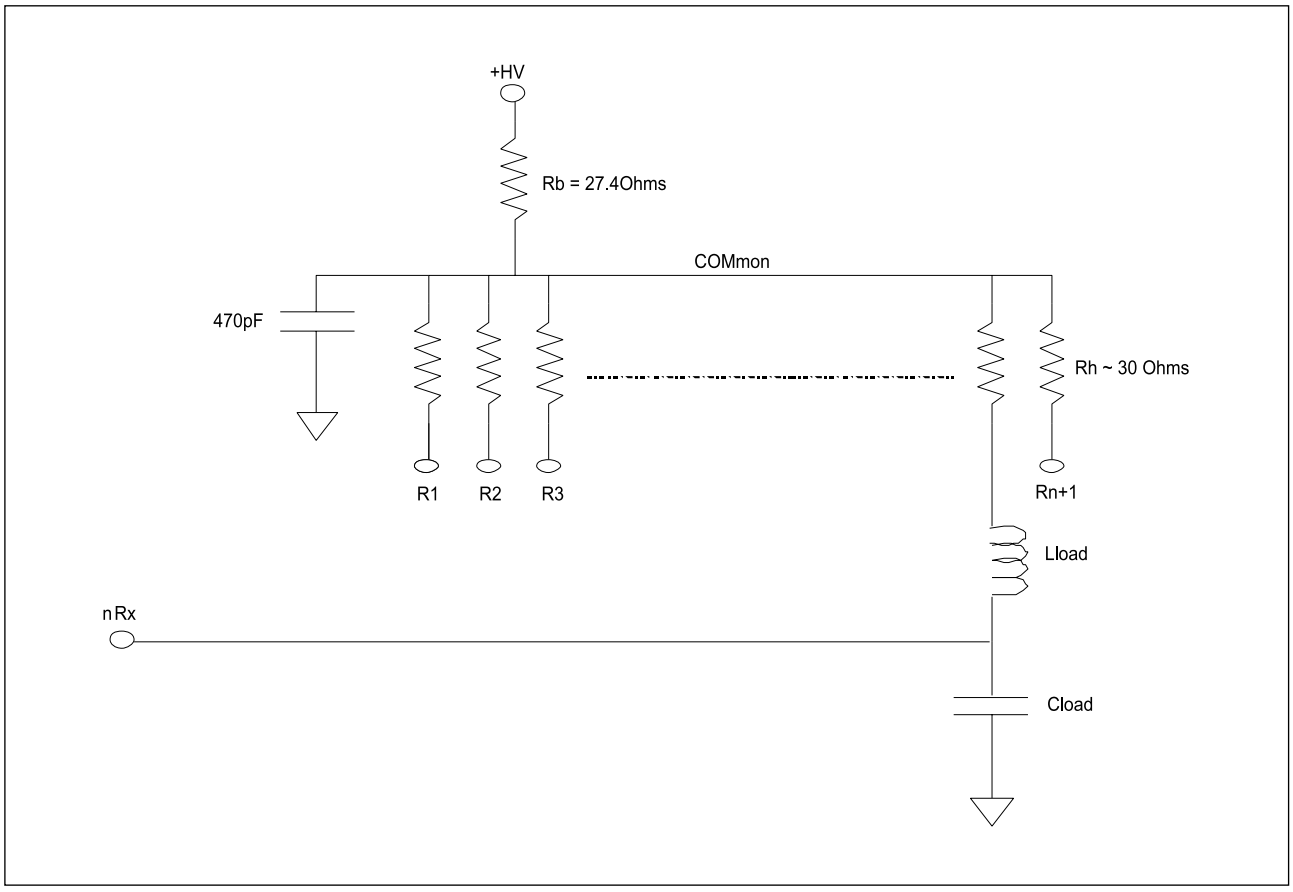
3.1.6.4 Power Driver Output Loading Schematic



<Figure 21. SIXSHOOTER Power Output Loading Schematic>

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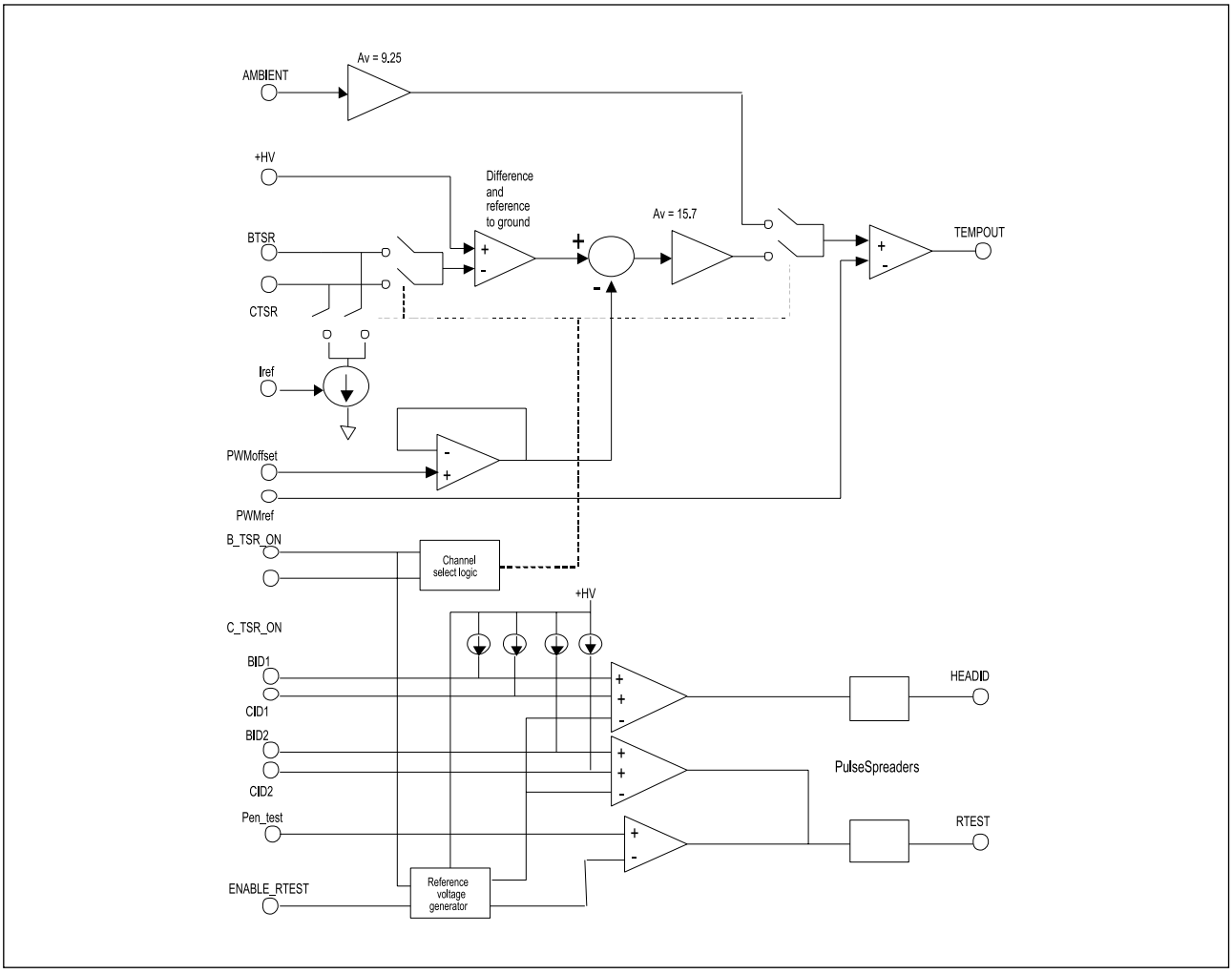
3.1.7 ERTE ASIC

3.1.7.1 General Information

The ERTE ASIC is driven by 19.2V, and consists of three functional blocks, such as the Head, the Pen ID which find out the kind of head by checking temperature and resistance difference when firing, and the Resistor Test which checks the possibility of the head firing.

3.1.7.2 ERTE Block Diagram



<Figure 22. Block Diagram of ERTE>

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3.1.8 FAX SENDING/RECEIVING PART

3.1.8.1 General Information

The circuit is for managing the transmitting signals of Modem and between the LIU part and Modem.

3.1.8.2 MODEM

There are two models, FM214 for the Basic model and FM 214-VS for the TAD model, which supports the Digital TAD and Speaker Phone. The Main PCB is designed for joint use in the Rhine. The modem has the single chip fax modem function and DTMF detection/DTMF signal generation function. The principal ports of the FM214 modem are as follows when using TAD Model. The LineOut (PIN69) is a port of the sending output from the modem, and the LineIn (PIN60) is a receiving input port. The Modem_RST (PIN115) is the signal from the CPU for initializing modem without system power off.D0~D7 are Data Bus, and RS0~RS4 is the signal for internal Register Selection of modem to decide mode. _MCS (PIN 91) is a signal of the Modem Chip, and _RD (PIN 92) and _WR (PIN 90) are control signals for a reading and writing. IRQ (PIN 108) is a signal for the Modem Interrupt Output. The transmitting speed of the FM214 is Maximum 14.4k bps.

3.1.8.3 SENDING PART

The circuit manages the sending output, which is analog signal of the modem.The output signal by each mode comes out from the modem lineout (PIN69), and it is sent out to PSTN telephone line via the Matching Transformer (600:600) of the LIU B'd.

3.1.8.4 RECEIVING PART

The analog signal from the Matching Transformer (600:600) of the LIU B'd is amplified at the LIU PBA, and the second amplification is at the main input part for inputting the signal in the LINEIN (PIN60) of receiving input part.

3.1.8.5 MIC INPUT PART (Not for the SF330 Basic Model)

SF335T Model has the Speaker Phone function and Tad function. For recording OGM and supporting a Speaker phone, MIC is needed. The first amplified signal at the OPE goes to the main and makes the second amplification. After that, it is inputted in the MIC (PIN61, 35) of modem.

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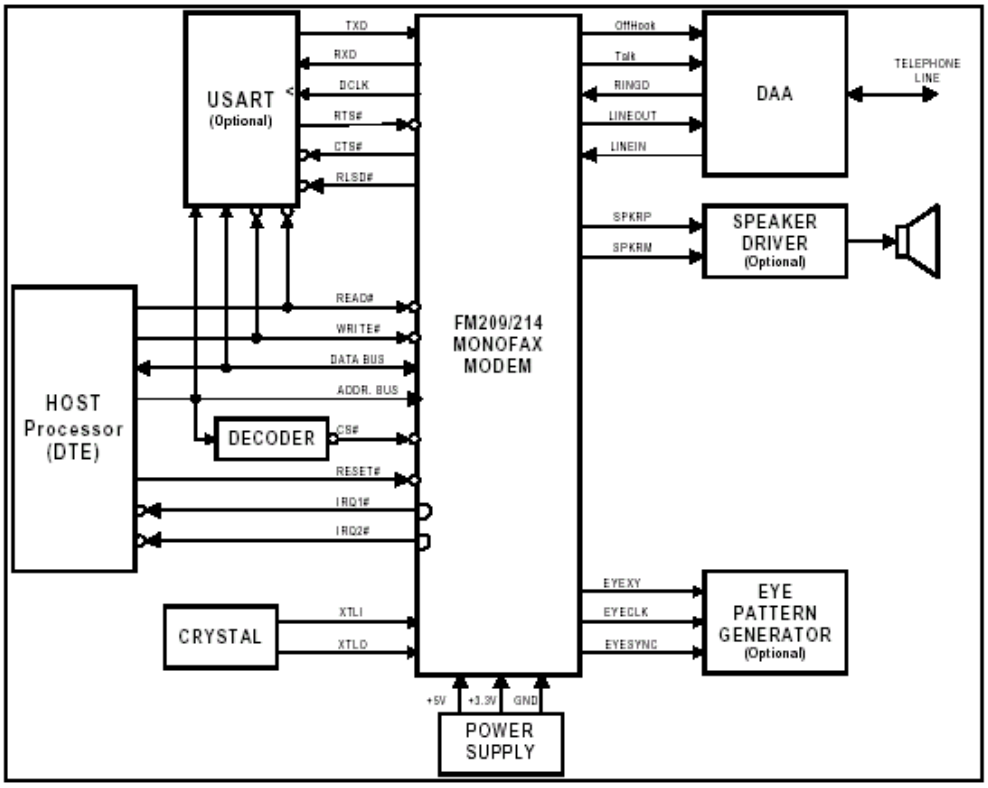
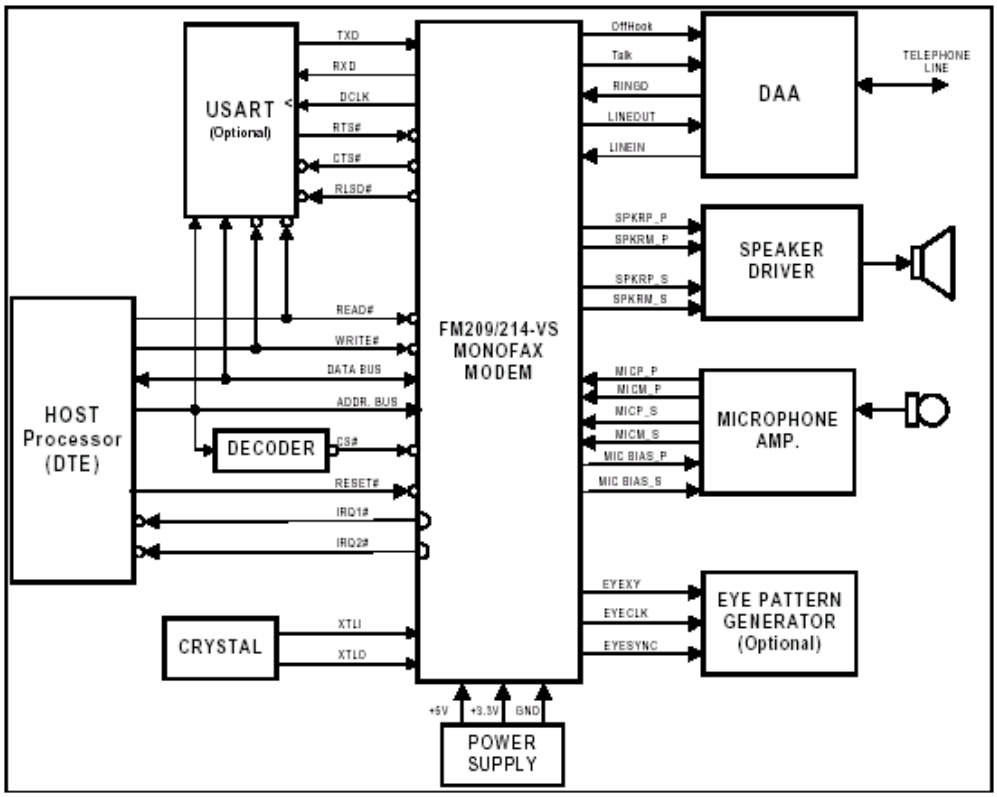
3.1.8.6 FM214 MODEM BLOCK DIAGRAM



3.1.8.7 FM214-VS MODEM BLOCK DIAGRAM



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3.1.8.8 FM214 SERIES MODEM PIN DESCRIPTION

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	SR4IN/RESERVED	MI	Modem Interconnect	51	MCLK_P	MI	Modem Interconnect
2	SR3OUT/RESERVED	MI	Modem Interconnect	52	CTRLSIN_P	MI	Modem Interconnect
3	EYESYNC	OA	Eye Pattern Circuit	53	RESERVED	MI	Modem Interconnect
4	EYECLK	OA	Eye Pattern Circuit	54	SOUT_P	MI	Modem Interconnect
5	RXD	OA	DTE serial interface	55	SIN_P	MI	Modem Interconnect
6	SR1IO	MI	Modem Interconnect	56	FSYNC_P	MI	Modem Interconnect
7	NC	-	No Connection	57	IARESET_P#	MI	Modem Interconnect
8	EYEXY	OA	Eye Pattern Circuit	58	AGND3	GND	IA Analog Ground
9	SR4OUT	MI	Modem Interconnect	59	NC	-	No Connection
10	VDD1	PWR	3.3V Digital Supply for DSP	60	LINEIN_P	I	Line Interface
11	RLSD#	OB	DTE Serial Interface	61	MICP_P	I	Microphone Input
12	DCLK	OB	DTE Serial Interface	62	MICM_P	I	Microphone Input
13	EN85#	IA	Host Parallel Interface	63	MICBIAS_P	O	Microphone Bias Output
14	GPI0	IA	Host Parallel Interface	64	NC	-	No Connection
15	RTS#	IA	DTE Serial Interface	65	NC	NC	No Connection
16	DGND1	GND	DSP Digital Ground	66	VREF_P	MI	Modem Interconnect
17	TXD	IA	DTE Serial Interface	67	VC_P	MI	Modem Interconnect
18	SA1CLK	MI	Modem Interconnect	68	VAA_P	PWR	5V Analog Supply for IA
19	RS4	IB	Host Parallel Interface	69	LINEOUT_P	O	Line Interface
20	RS3	IB	Host Parallel Interface	70	AGND4	GND	IA Analog Ground
21	RS2	IB	Host Parallel Interface	71	SPKRP_P	O	Speaker Interface Output
22	RS1	IB	Host Parallel Interface	72	SPKRM_P	O	Speaker Interface Output
23	RS0	IB	Host Parallel Interface	73	AVDD_P	PWR	3.3V digital power for IA
24	YCLK	I		74	NC	-	No Connection
25	IACLK	MI	Modem Interconnect	75	ICLK_P	MI	Modem Interconnect
26	IA1CLK	MI	Modem Interconnect	76	MCLK_S/NC	MI	Modem Interconnect
27	CTRLSIN_S/NC	MI	Modem Interconnect	77	VDD2	PWR	3.3V Digital Supply for DSP
28	RESERVED/NC	MI	Modem Interconnect	78	D7	IB/OC	Host Parallel Interface
29	SOUT_S/NC	MI	Modem Interconnect	79	D6	IB/OC	Host Parallel Interface
30	SIN_S/NC	MI	Modem Interconnect	80	D5	IB/OC	Host Parallel Interface
31	FSYNC_S/NC	MI	Modem Interconnect	81	D4	IB/OC	Host Parallel Interface
32	IARESET_S#/NC	MI	Modem Interconnect	82	D3	IB/OC	Host Parallel Interface
33	AGND1	GND	IA Analog Ground	83	D2	IB/OC	Host Parallel Interface
34	LINEIN_S/NC	I	Line Interface	84	DGND2	GND	DSP Digital Ground
35	MICP_S/NC	I	Microphone Input	85	VDD3	PWR	3.3V Digital Supply for DSP
36	MICM_S/NC	I	Microphone Input	86	D1	IB/OC	Host Parallel Interface
37	MICBIAS_S/NC	O	Microphone Bias Output	87	DGND3	GND	DSP Digital Ground
38	NC	-	No Connection	88	D0	IB/OC	Host Parallel Interface
39	NC	-	No Connection	89	CSBR#	IB	Host Parallel Interface
40	VREF_S/NC	MI	Modem Interconnect	90	WRITE#	IB	Host Parallel Interface
41	VC_S/NC	MI	Modem Interconnect	91	CS#	IB	Host Parallel Interface
42	VAA_S/NC	PWR	5V IA Analog power	92	READ#	IB	Host Parallel Interface
43	LINEOUT_S/NC	O	Line Interface	93	GPI2	IA	General purpose input
44	NC	-	No Connection	94	GPI3	IA	General purpose input
45	AGND2	GND	IA Analog Ground	95	GPI4	IA	General purpose input
46	SPKRP_S/NC	O	Speaker Interface Output	96	GPI5	IA	General purpose input
47	SPKRM_S/NC	O	Speaker Interface Output	97	GPI6	IA	General purpose input
48	AVDD_S/NC	PWR	3.3V digital power for IA	98	GPI7	IA	General purpose input
49	RESERVED/NC	MI	Modem Interconnect	99	GPO7	OC	General purpose output
50	ICLK_S/NC	MI	Modem Interconnect	100	VDD4	PWR	3.3V DSP Digital Power

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
101	GPO6	OC	General purpose output	115	RESET#	IB	External reset
102	GPO5	OC	General purpose output	116	XTALI	I	Crystal in
103	RESERVED	MI	Modem Interconnect	117	XTALO	O	Crystal Out
104	GPO4	OC	General purpose output	118	RESERVED	MI	Modem Interconnect
105	GPO3	OC	General purpose output	119	XCLK	OB	X clock output
106	DGND4	GND	DSP Digital Ground	120	GPI1	IA	General purpose input
107	CTS#	OB	DTE Serial Interface	121	IRQ2#	OA	Interrupt request
108	IRQ1#	OB	Interrupt request	122	SR3IN	MI	Modem Interconnect
109	GPO2	OC	General purpose output	123	RESERVED	MI	Modem Interconnect
110	GPO1	OC	General purpose output	124	RESERVED	MI	Modem Interconnect
111	GPO0	OC	GPO0 (IAreset)	125	DGND6	GND	DSP Digital Ground
112	VDD5	PWR	3.3V DSP Digital Power	126	DVAA	PWR	3.3V DSP analog power
113	VGG	PWR	5V DSP Digital	127	AGND5	GND	DSP Analog Ground
114	DGND5	GND	DSP Digital Ground	128	RESERVED	MI	Modem Interconnect

Notes:
I/O types:
MI = Modem interconnect.
IA, IB, = digital input (see Table 2-3).
OA, OB, OC = digital output (see Table 2-3).
I = analog input (see Table 2-4).
O = analog output (see Table 2-4).
_P Signals: Primary IA
_S Signals: Secondary IA
Reserved = No external connection allowed.

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3.2 OPE

3.2.1 Basic Concept

3.2.1.1 Overview

OPE BOARD is separated from the Main Board functionally, and operates entire Micom(HT48C5A-000Z) in the Board. OPE and Main exchange mutual information using UART(universal asynchronous receiver/transmitter) channel. Also, Resetting of OPE is designed to control at the Main. Micom in OPE performs key-scanning and LCD, LED display control, and senses document detect, Scan position and so on. When information is generated from OPE(key touch, sensor level change, etc.), it sends specific code coping with the situation to Main, and the Main operates system by analyzing this code. If the Main tries to display data on OPE, the Main sends data to OPE via UART line on the basis of the format specified, and OPE displays it to LCD.

In the case of the TAD Model, the MIC for the Speaker Phone and OGM and the Pre-Amp part of the MIC have built-in at OPE circuit.

3.2.1.2 UART

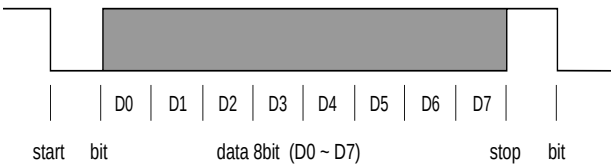
OPE and MAIN exchange information mutually by using asynchronous communication mode(UART), and in full duplex. Band rate is 9600bps, and uses 7.37MHz resonator as oscillating element. It engages in communication with 8bit data without parity bit. UART line has two lines for Tx and Rx, and the default level is in the 'high' state. For communication, the start bit(low level) is transmitted before 8bit data. When the data transmission(8bit) is completed, the high state is maintained as the stop bit(high level) is transmitted. Data is transmitted from LSB(DO), and MSB(D7) is transmitted lastly.

3.2.2 UART Operation

3.2.2.1 UART Communication

<1> UART TX FORMAT

Codes for change of KEY, TOUCH, SENSOR LEVEL and so on are transmitted in single code without PRE/POST DATA, and OK or Error messages to check if communication is performed properly are also transmitted in single code. Provided that, in case the Main requested a certain value(LCD, other register) particularly, data requested is transmitted followed by sending Post Data('EOH') first.



<2> UART RX FORMAT

Data being received will be arranged to be received according to the following specified format to know what data they are.

a)	Type of data received
b)	Number of data (N+1) received after.
	----------
	c) DATA(N)
	----------
d)	Check sum(1)

DATA are received in the sequence of A,B,C, and D, and the Check sum to check if the transmission is made properly will be found by doing XOR data from A to C.

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3.2.2.2 UART communication DATA

<1> UART transmission DATA(received by the Main side)

Types	STATUS	USED PORT	LEVEL	REMARKS
key data	ON	PORT PC0~PORT PC7	L	
	OFF		H	
SCAN POSITION sensor	ON	PORT PB3	H	MAGIC not applied
	OFF		L	
DOC. detector sensor	ON	PORT PB-5	L	MAGIC not applied
	OFF		H	
For initial use of initial OPE				After power on, generated only once
UART communication	OK			(Note 2)
	ERR			
LCD interface of OPE	OK			When failed in the interface once & when succeeded first(Note 2)
	ERR			
Self initial generation of OPE				LCD data keeps status quo
Send data requested by the Main				Data types:LCD, other(Note 3)

<Note> 1. After this, keep waiting until there is response from the Main.
2. The case of longer time(longer than 10ms) elapsed longer than waiting time required for Interface is regarded as fail.
3. After this code went out, then data requested it goes out.

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<2> Received DATA(transmitted by MAIN)

1. DATA TYPE

DATA types	Meaning	Remarks
a1 H	LCD DISPLAY DATA(FULL LINE)	
a4 H	LED DATA	

2. NO. OF DATA

• In case DATA is N BYTE, N+1

3. DATA

In case DATA TYPE is LCD DATA, it is configured with ASCII CODE to be displayed.
In case DATA TYPE is LED DATA, it is 1 BYTE.

• LED DATA BIT ASSIGNMENT :

DATA BIT	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
LED NO.	LED 0	LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7
	Answer LED	Ink Save LED	Silent Mode LED	not used				

4. CHECK SUM

The value done XOR all of them from DATA TYPE to DATA.

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3.2.3 I/O PORT configuration and use usage

It has 32 I/O Ports, and 24 Ports of them are arranged to decide I/O direction with Software Control, and the rest 8 Ports are arranged to be used for Input or Output only. All of I/O Ports are classified into four Blocks according to the characteristics of I/O Control, and each Block consists of 8 Ports.

Type	I/O Control	I/O direction	USE	Remarks
PA X	Byte Control	I/O => Output	LED Control	Used as LCD VCCCONTROL in MAGIC.
PB X	Byte Control	In : 4, Out : 4	UART, LCD, Sensor	MAGIC SENSOR not applied.
PC X	Byte Control	I/O => Input	Key Input	
PD X	Byte Control	I/O => Output	LCD Data, Key Scan	

<1> Assignment of Port PAX

- PA1 : ANSWER LED (RED)
- PA2 : INK_SAVE LED (GREEN)
- PA3 : NIGHT_MODE LED (GREEN)
- PA4 : RESERVED
- PA5 : SRESERVED
- PA6 : RESERVED
- PA7 : RESERVED

* HIGH --> LED OFF
LOW --> LED ON

<2> Assignment of port PBX

- PB0(Output) : LCD Enable
- PB1(Output) : LCD R/W
- PB2(Output) : LCD RS
- PB3(Input) : GND
- PB4(Input) : Unused (Pull-up)
- PB5(Input) : GND
- PB6(Output) : UART TXD in Main UART
- PB7(Input) : UART RXD from Main UART

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3.3 LIU B'd

3.3.1 GENERAL DESCRIPTION

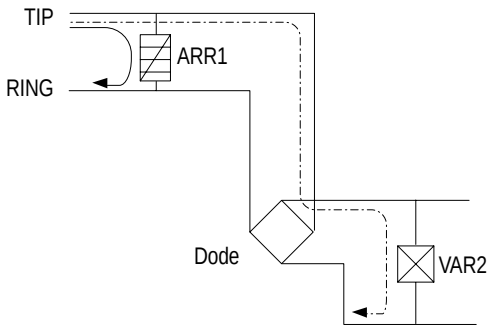
LIU (Line interface unit) is consist of Tel-line interface part and FAX/Speech part.

<1> TEL LINE INTERFACE PART

- Surge and over voltage protection part
- Remote circuit
- Ring detector circuit
- Ext phone detector circuit
- DCR and Impedance matching circuit

1. Surge and over voltage protection circuit.

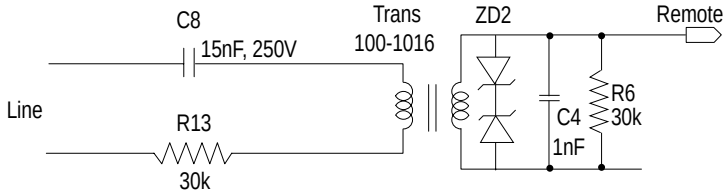
- ARR1 component is the protection of lightning surge. (Spec : 400V ± 20% , 500A)
- VAR2 is a varistor that decrease over voltage noise. (Spec : 82V , 1250A)



- Over 400V of high voltage is decreased by ARR1 and the rest voltage
- (low voltage : 400V under level) is decreased by VAR2.

2. Remote circuit

- C8, R13 use for DC coupling / On-hook impedance.
- Over voltage is depressed by ZD component
- DTMF Detector path for Local start (SF-330/331P)
- Caller ID Signal path



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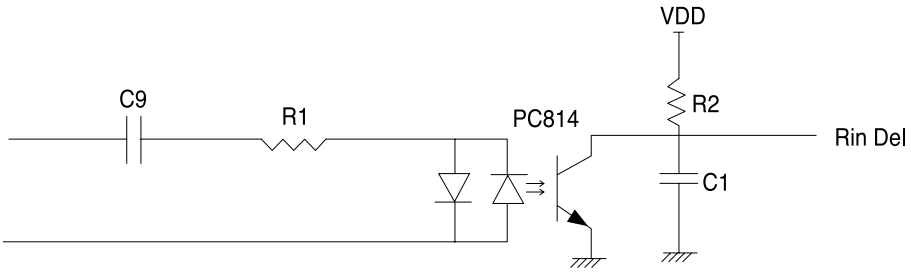
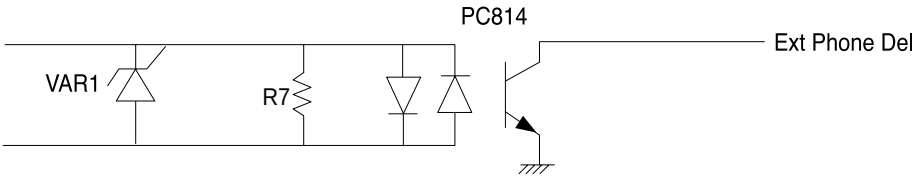
3. Ring detector circuit

- C9 use for DC coupling and Ring impedance (Ring impedance spec : Min 4Kohm)
- R1 (1/ 1W)protect overvoltage into PC814.
- Ring signal transfer from 1st circuit to 2nd circuit through PC814
- R2/C1 translator to recognize for ring signal.



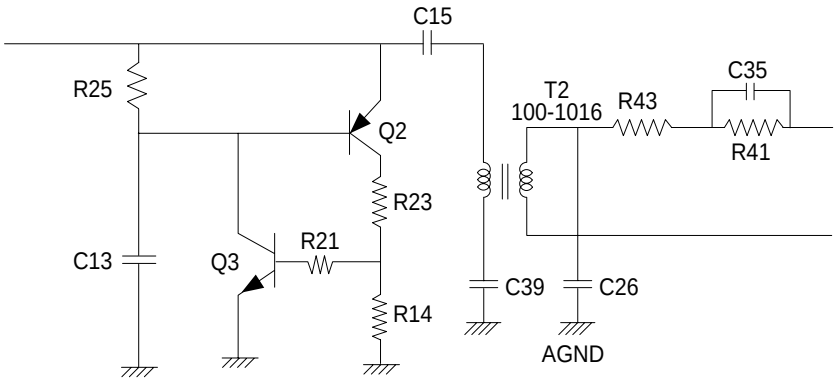
4. Ext hook detector circuit

- SF-330/331P model have Ext-phone jack to connect TAM or external phone.
- VAR1 protect overvoltage into PC814.
- R7 is marching component of Ext phone for detect another normal phone.



5. DCR / Current limit circuit / impedance

- DCR / Current limit circuit consist of R25, C13, Q2, Q3, R21, R23, R14.
- Current limit circuit apply only EU nation.(Q3, R21)
- Impedance circuit consist of T2, C26, R43, R41, C35.



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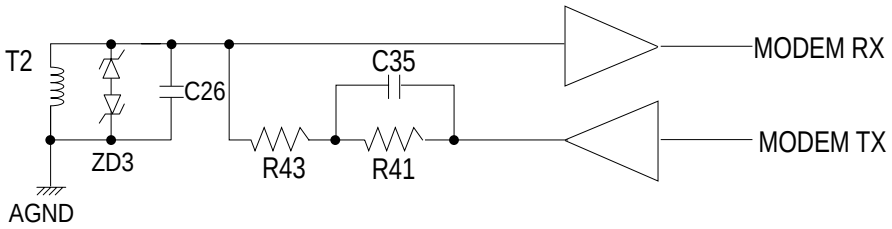
<2> Fax / Speech part

- Fax TX / RX circuit
- Speech part (Handset MIC / RECEIVE)

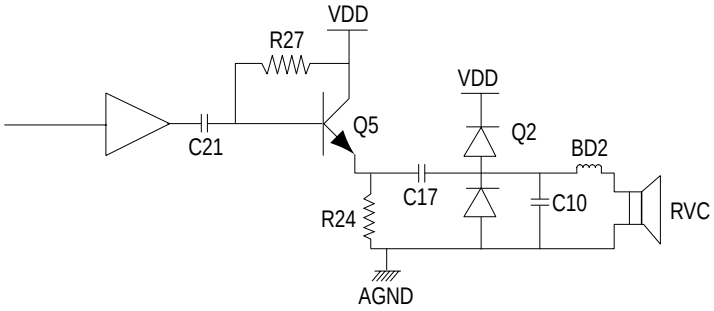
1. FAX TX / RX circuit

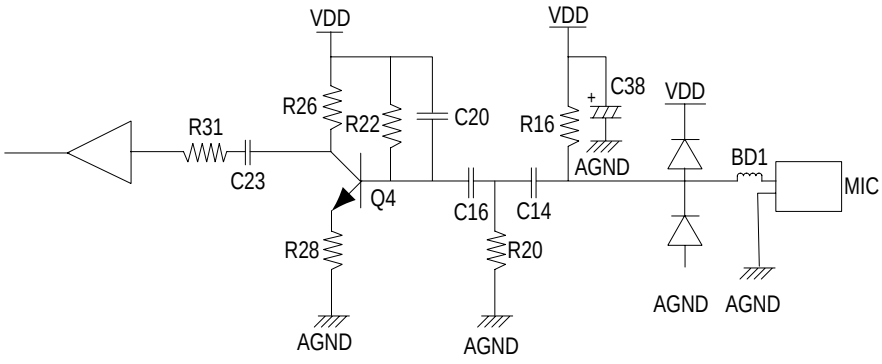
- DTMF / OGM (335T) and Fax tone transmit from Modem tx part → impedance matching part (R43, C35, R4) →T1 trans → tel-line.
- Dial tone / ICM (335T) and Fax tone transmit form tel-line → T1 trans → Modem rx part.



2. Speech part (Handset MIC / Receive)

- Handset Receive





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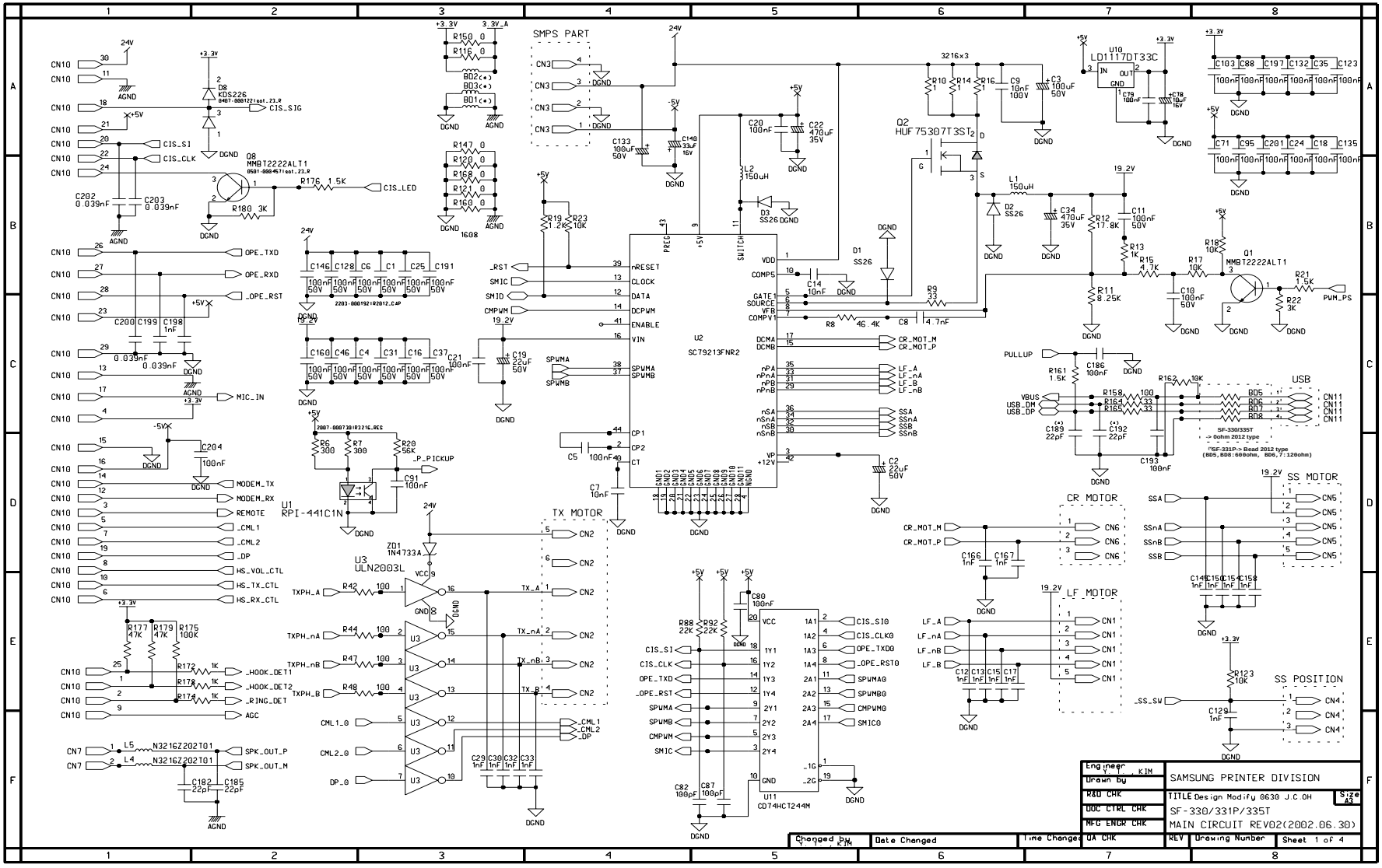
4. Schematic Diagrams

4-1 Main Circuit Diagram (1/4)



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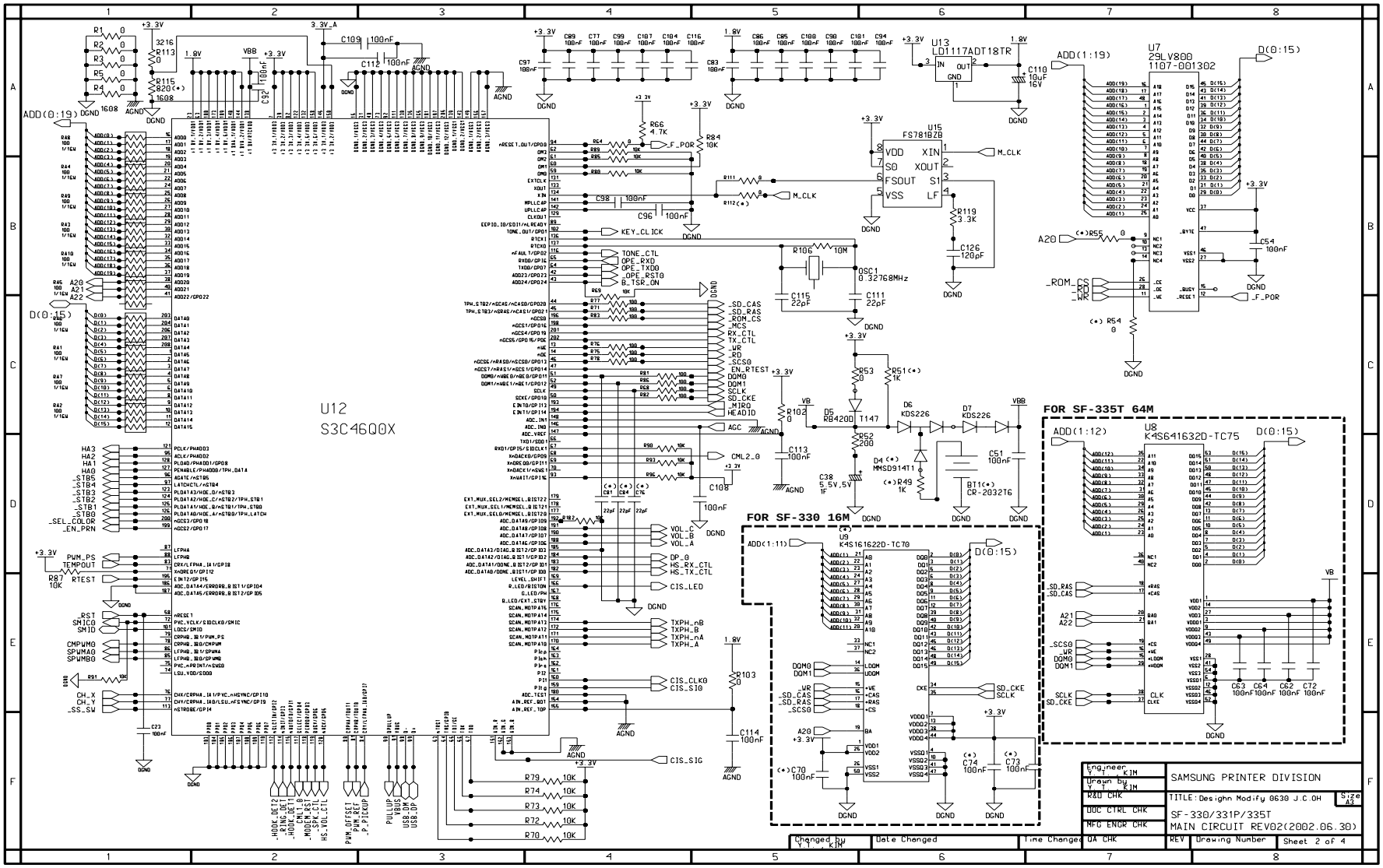
Main Circuit Diagram (2/4)



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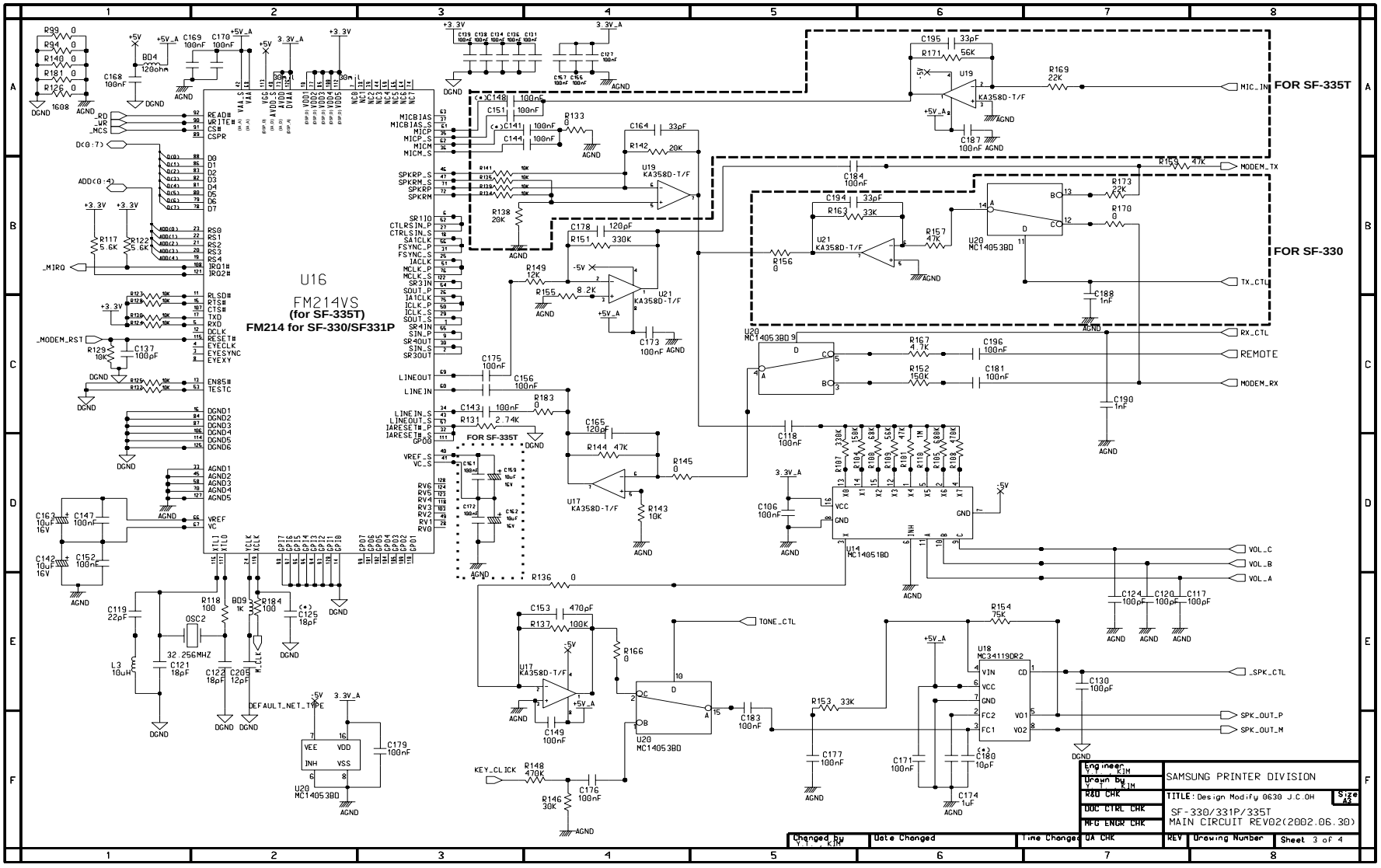
Main Circuit Diagram (3/4)



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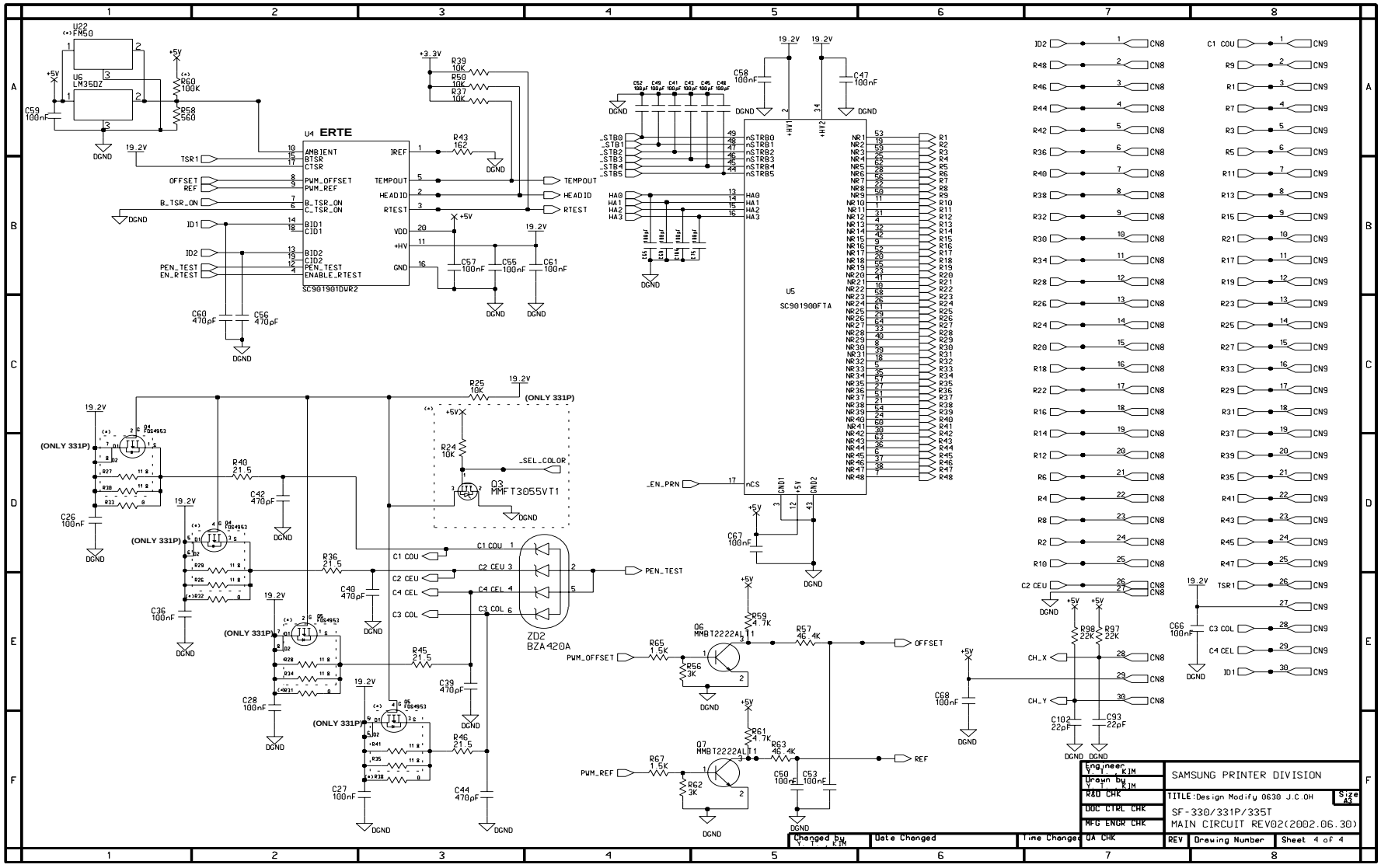
Main Circuit Diagram (4/4)



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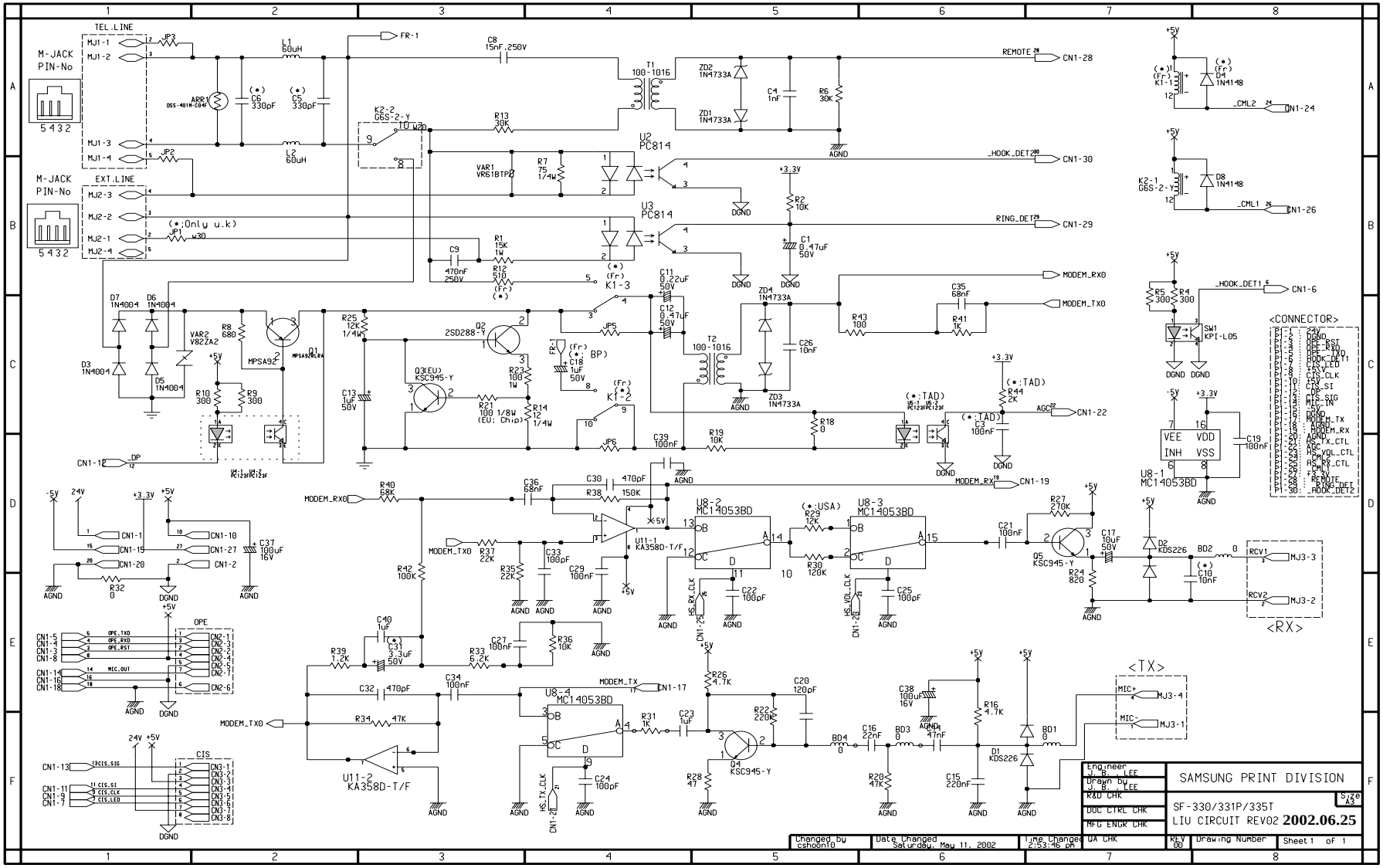
4-2 LIU Circuit Diagram



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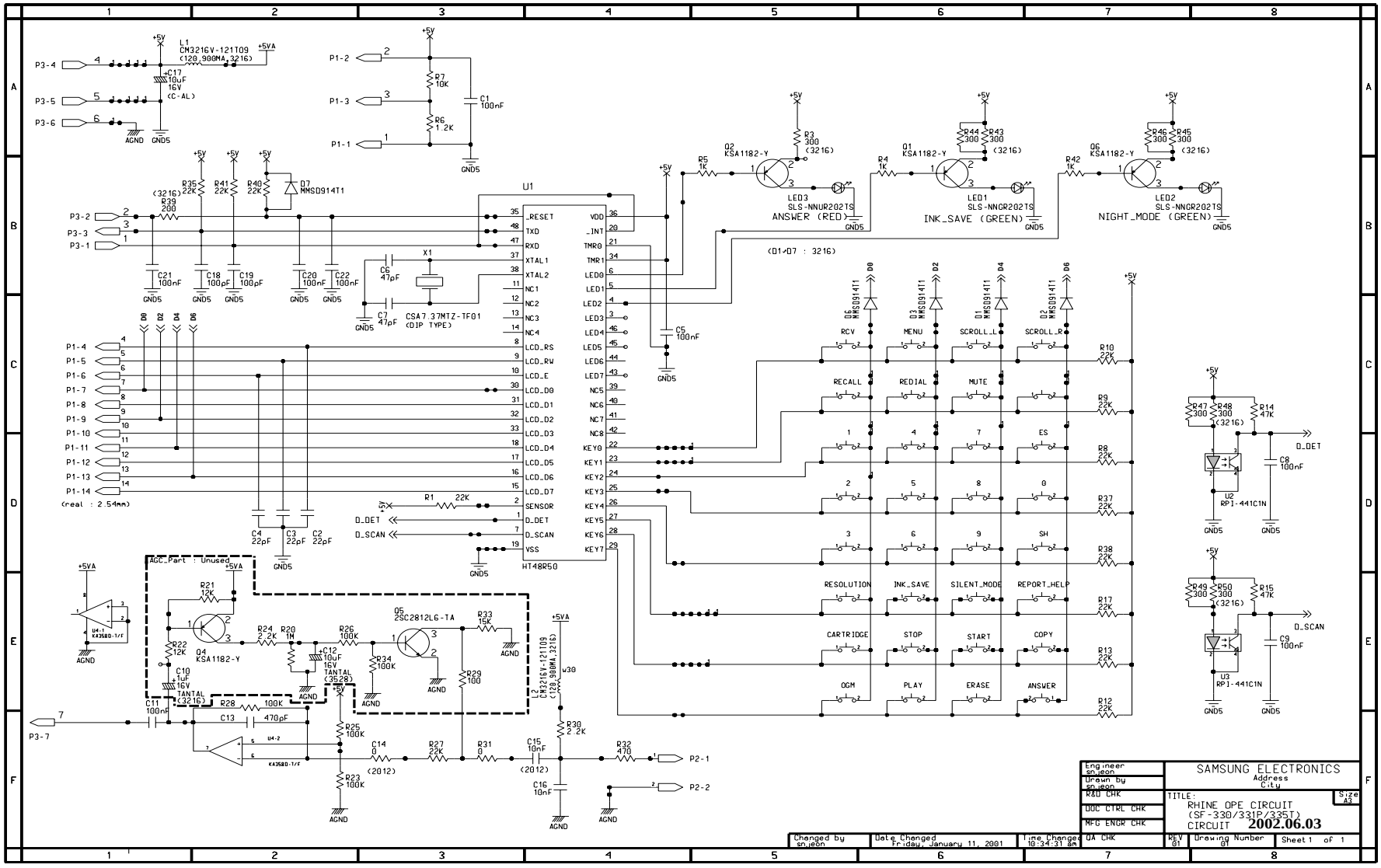
4-3 OPE Circuit Diagram



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